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DEVELOPMENT OF RELIABILITY METHODOLOGY

FOR SYSTEMS ENGINEERING

Volume II. Application: Design Reliability Analysis of a
250 volt-ampere Static Inverter

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FOREWORD

This is one of three volumes of the final report prepared by Research Triangle Institute, Durham, North Carolina under NASA contract NASw-905, "Development of Reliability Methodology for Systems Engineering". This work was administered under the technical direction of the Office of Reliability and Quality Assurance, NASA Headquarters with Mr. John E. Condon, Director, as technical contract monitor.

The effort under this contract began in April 1964, to continue for approximately two years and was performed jointly by personnel from the Institute's Solid State Laboratory and Statistics Research Division. Dr. R. M. Burger was technical director with W. S. Thompson serving as project leader. C. D. Parker was a principal contributor to this report with A. C. Nelson assisting in the analyses.

A static inverter designed by the Applied Research Branch, Astrionics Laboratory, George C. Marshall Space Flight Center, NASA, Huntsville, Alabama, was selected to test the analysis techniques and procedures described in Vol. I of this report. Permission to use this system in the contract study is appreciated. Special thanks are given to R. F. Harwell, W. J. Kreider, A. E. Willis, J. M. Gould and C. E. Winkler of the Astrionics Laboratory for their helpful discussions on the inverter operation and design. Even though this study did not allow a complete analysis of the inverter, it is hoped that the results obtained will help in its development.

PREFACE

The objective of this contract was to develop reliability methodology which relates to various techniques which can be applied in designing reliable systems and to extend the methodology by the development and demonstration of new techniques. It was important to have available a system on which to test and demonstrate the results. A complex static inverter was chosen for this purpose and served this role well.

The three major areas of effort in the program are defined by the titles of the final report volumes listed as follows:

Vol. I. Methodology: Analysis Techniques and Procedures

Vol. II. Application: Design Reliability Analysis of a 250 Volt-Ampere
Static Inverter

Vol. III. Theoretical Investigations: An Approach to a Class of Reliability
Problems

The purpose of Vol. I is to describe the mathematical techniques which are available for performing the reliability analysis of equipment life and performance. Appropriate technique selection, coupled with proper coordination of efforts during design, are essential for engineering reliability into equipment. Vol. II considers the practical application of reliability analysis to circuit design and demonstrates improvements in the identification and solution of problems using the techniques described in Vol. I. This employs the static inverter as an example. Vol. III describes fundamental studies in stochastic processes related to reliability.

Other technical reports issued under this contract effort are as follows:

1. "On Certain Functionals of Normal Processes," Technical Report No. 1, September 1964.
2. "Functional Description of a 250 Volt-Ampere Static Inverter," Technical Report No. 2, December 1964.
3. "The Variance of the Number of Zeros of Stationary Normal Processes," Technical Report No. 3, March 1965.
4. "Problems in Probability," Technical Report No. 4, October 1965.
5. "Reliability Analysis of Timing Channel Circuits in a Static Inverter," Technical Report No. 5, December 1965.
6. "Reliability Analysis of Timing Channel Circuits in a Static Inverter," Technical Report No. 6, January, 1966.

ABSTRACT

This report describes the application of design stage reliability analyses to a static inverter, emphasizing the use of improved analytical techniques as a supplement, but not a substitute, to conventional analyses. Models are used to relate the important performance characteristics to the factors that influence their variation. As a means to achieving the most reliable design within practical constraints, emphasis is on identifying and implementing design improvements rather than on obtaining a number to represent reliability. Performance variation analyses, reliability prediction, component stress analyses, and failure modes and effects analyses individually contribute to reliability; however, it is through the proper coordination of these tasks and appropriate combination and interpretation of their results that the earliest assurance for reliable design is achieved. Several significant design problems were detected with this approach that conventional analysis could overlook.

TABLE OF CONTENTS

FOREWORD	Page ii
PREFACE	iii
ABSTRACT	iv
1. Introduction	1
2. Preliminary Design Considerations	3
2.1 Statement of the Design Problem	3
2.2 Preliminary Design Analyses	5
3. Design Stage Analyses	6
3.1 Analysis Method	6
3.2 Functional Analyses	7
3.2.1 Mission Definition	9
3.2.2 Interface Characteristics	12
3.2.2.1 Outputs	12
3.2.2.2 Inputs	16
3.2.2.3 Loads	18
3.2.2.4 Environmental Factors	20
3.2.3 Reliability Considerations for the Inverter Design	22
3.2.4 Functional Breakdown for Analysis	25
3.3 Quantitative Analyses	29
3.3.1 Analyses for the Complete Circuit	29
3.3.1.1 Reliability Prediction	29
3.3.1.2 Failure Modes and Effects Analyses	33
3.3.1.3 Component Stress Analyses	35
3.3.1.4 Performance Variation Analyses	36
3.3.2 Analyses for Circuit Sections	54
3.3.2.1 Timing Section	55
3.3.2.2 Control and Conversion Section	56
3.3.3 Analyses for Major Circuits	57
3.3.3.1 Timing Generators A and B	57
3.3.3.2 Voltage Regulation Loop	57
3.3.3.3 Overcurrent Protection Loop	90
3.3.4 Analyses for Small Circuits	93
3.3.4.1 Six-volt dc Regulated Supply	94
3.3.4.2 Electronic Switches	96
3.3.4.3 Primary Oscillators	101
3.3.4.4 Frequency Countdown Circuits	102

TABLE OF CONTENTS (continued)

	Page
3.3.4.5 Clock Pulse Amplifiers	105
3.3.4.6 Pulse Sequence Generators	106
3.3.4.7 Coupling Circuits	110
3.3.4.8 Timing Pulse Amplifiers	112
3.3.4.9 Power Converters	115
3.3.4.10 Output Circuit	121
3.3.4.11 Voltage Error Detection Circuit	122
3.3.4.12 Overcurrent Detection Circuit	123
3.3.4.13 20-volt dc Regulated Supply	125
3.3.4.14 Magnetic Amplifier Driver Circuit	126
3.3.4.15 Magnetic Amplifier Circuit	129
3.3.4.16 Primary Voltage Regulator	137
3.4 Design Stage Analysis Conclusions and Recommendations	142
4. Later Stage Considerations	152
4.1 Experimental Model	152
4.2 Production	154
5. Conclusions with Regard to the Analysis Approach	155
6. References	157
APPENDICES	
A. Output Circuit Equations	158
B. Voltage Regulation Loop Equations	163
C. Failure Modes and Effects Analysis Summary	166
D. Equations for Harmonic Distortion Analysis	175
E. Component Stress Analysis Summary	182
F. Inverter Parts List	193
G. Summary of Observed Failures	197

1.0 Introduction

System reliability is a universal goal in engineering even though it is, at times, subverted to cost, performance, or delivery schedule. In space research, the premium on reliability is magnified. New methods are continually sought for proving and improving reliability. With the considerable technological advances in space systems, a priori confidence in the achievement of mission success has become increasingly difficult to obtain. Only minor significance can be attached to reliability predictions because of the many simplifying assumptions and imprecision in data. Still, the need for assurance of mission success exists.

A more realizable goal is design improvement as stimulated by objective assessment. A design modification is identified, implemented, and then evaluated on a comparative basis. Again, however, system complexity and the number of factors which affect system operation necessitate a cautious approach to this process. Examples of design modifications which were intended to improve reliability but which had the opposite effect are not rare.

The engineer is thus receptive to new analytical methods which enhance his ability to evaluate designs and discriminate between alternate approaches. In Volume I of this report, analytical methods for evaluating system reliability were discussed with emphasis on variations in performance and on reliability-life techniques. These methods are not, in themselves, new but the perspective in which they are presented and the details of their use are directed toward practical utility. This utility, and its limitations, are the concern of this volume of the report. The analysis techniques are applied to an electronic equipment so as to supplement, but not to replace, conventional design and analysis methods.

The equipment on which these techniques have been tested is a static inverter being developed at the George C. Marshall Space Flight Center as a highly-reliable, general-purpose ac power supply for space applications. The approach used in the studies was to seek potential weak points in the design and to evaluate approaches for strengthening these. Since the static inverter is very well designed, it was to be expected that few weaknesses would be found. It was also expected that, since thorough analysis has been performed on the static inverter, the identification of weaknesses would be a critical test of the analytical methods. The analysis was focused at the equipment design stage since it is at this stage of development when changes are most readily included.

The analysis of any system requires intimate familiarity with its design and operation. To this end a thorough analysis of the static inverter has been carried out. Initially, a detailed description of the circuit operation was prepared

[Ref. 1] and will be frequently referenced in the text of this report. A preliminary engineering analysis was next performed [Ref. 2] and identified certain problem areas for more thorough investigation. One special study [Ref. 3] treats some timing circuits in the inverter. One essential element of the complete analysis is an experimental breadboard model of the system. This has been exhaustively exercised to produce data and test hypotheses.

The contents of this volume are concentrated in Section 3. This contains the circuit design analysis, and related conclusions and recommendations are presented in Section 3.4. For overall perspective Section 2 describes in brief some typical preliminary design considerations leading to the present configuration, and similarly, Section 4 describes applications of analyses to later stages of the equipment development process. Conclusions with regard to the analysis approach are given in Section 5.

A readily apparent comment with respect to the work reported here is that, to a considerable extent, it is no more than good engineering. This, however, is the goal of reliability analysis; to achieve good engineering in a complex environment. Analysis is thus employed primarily to discern those aspects of design on which to focus effort and to insure that the design is comprehensive. It is hoped that the results described here demonstrate the value of thorough analysis in improving system reliability. There is no attempt to substantiate this with numbers to represent actual reliability since these have limited meaning for a complex system.

Because the static inverter study was only a portion of the total effort, a complete analysis of the inverter was not possible. For example, the transient response studies are in the form of a status report. In such cases the analysis is described, available results reported, and recommendations for further effort presented. In addition, the effort was not coordinated directly with the actual development schedule. Design modifications by the design group were, however, introduced into the analysis when feasible. It is hoped that considerable benefit for improvements in the actual design will result.

The conclusions of this study of the static inverter are positive. The analysis has aided in distinguishing the merits of alternate approaches; it has identified a number of valuable design modifications which led to a better system; it has provided increased assurance that the system will perform as intended; and it has tested the analytical methods. Apparent now is the value of a failure modes and effects analysis, performed early in the development cycle, in directing subsequent analytical studies in performance variation analysis, stress analysis, and reliability prediction, to the portions of the system for which they will prove most useful.

2.0 Preliminary Design Considerations

Due to the emphasis on design stage analyses presented in Section 3, this section is brief, and is included to assist in defining the scope of a thorough analysis for reliability and the interrelationship of preliminary design considerations to analyses during later stages of equipment development. As a starting point for the analysis a design problem statement is first presented in Section 2.1 and is written from the viewpoint of a technical manager of the cognizant design group for the static inverter. Section 2.2 presents a discussion of some specific preliminary design problems the solution of which contribute to a reliable design of the inverter.

2.1 Statement of the Static Inverter Design Problem

In considering space exploration systems, the need for compact, long-life, highly-reliable dc to ac converters is apparent. Rotating machinery is still relied on for power conversion in some applications. With advances in solid state electronics, static inverters exhibit higher efficiency, higher reliability, smaller size and less weight, than rotory inverters. Their capability for delivering high powers, extending into the kilowatt range, has been demonstrated.

A 450 volt-ampere static inverter has been developed and is in production. It is being used in the Saturn I system. In this inverter, power conversion is provided by six identical power converter stages which employ transistors as power switches. These switch sequentially at 400 cps yielding a train of six square waves. The simultaneous summation of these six square waves yields a stepped waveform which approximates a sinusoid. Low pass filtering of this step waveform attenuates the harmonics to provide a near sinusoidal output. The switching sequence of the power converter stages is controlled by timing signals derived from the output of six flip-flop circuits interconnected to form a ring counter. The clock pulse controlling this timing operation is provided by a crystal controlled oscillator.

Voltage control of the inverter output is provided by a feedback loop which utilizes a magnetic amplifier as the main control device. In the loop operation the output voltage is compared to a reference voltage to generate an error signal. This error signal is applied as a current to the control winding of the magnetic amplifier. The output of the magnetic amplifier is a pulse-width modulated rectangular wave having a duty cycle proportional to the voltage error. The magnetic amplifier output signal thus derived serves as the control for modulating the unregulated dc input. The modulated dc is filtered and then applied to the power converter stages.

With this inverter design, the output voltage is regulated within ± 1.0 vac rms over the full load range of 0 to 450 va and with input voltage variations from 25 to 30 vdc. Harmonic distortion of the output waveform is held to less than 5%. The weight of the complete inverter package is less than 40 pounds and its efficiency is approximately 70%. The adequacy of the design concept employed for meeting such requirements are thus well established.

The proven performance of this inverter coupled with the projected need for ac power supplies for future space systems suggests that effort would be worthwhile in improving this design by incorporating available state-of-the-art features. For example, advances in solid state techniques have led to the development and availability of highly reliable integrated circuits as possible replacements for some of the conventional circuits. These exhibit a competitive advantage over the conventional circuits in both reliability and size. Even though cost may temporarily be greater, it is not prohibitive. Since the timing section uses digital logic for which integrated circuits are available this is given first consideration. Integrated circuits for other portions of the inverter circuitry are not now available but are being developed.

With the redesign justified other improvements can be considered. These include the use of improved conventional components and reliability improvement through redundancy. In the existing design the overcurrent protection is provided by one-shot fusing. Feedback control for providing recoverable overcurrent protection is possible and has distinct advantages.

There is a trend towards standardization of system components and modularization of systems to permit maximum use of off-the-shelf type components. In developing an improved version of the static inverter it is desirable to produce an equipment that is in keeping with this trend. An inverter having a lower power capability is a more versatile ac power supply in the framework of this standardization concept. For typical system functional blocks, a power supply capability of 250 va is near optimum. A compact inverter having this power capability and which is highly reliable in all of the many environments in which it may be operated, may be useful in many space systems as a standard off-the-shelf hardware item.

The design problem is to develop a reliable general purpose static inverter which converts dc power at 25 to 30 vdc to three-phase, ac, sinusoidal, 400 cps, 115 vac rms with a power capability of 250 va employing the major design concepts of the existing 450 va static inverter.

2.2 Preliminary Design Analyses

To achieve maximum reliability in an equipment, reliability studies should begin with the conception and continue through the development to the final operational form. Analyses during the early stages are limited in depth, due to the uncertainties that exist prior to the designation of specific hardware for which application data is available. However, realistic analyses can be performed during preliminary design which determine the feasibility of design approaches and which identify trade-offs among the different designs. Preliminary design considerations applicable to the inverter are listed as follows:

- Comparing rotating conversion equipment to static inversion.
- Applying integrated circuits to low-power switching.
- Investigating possible redundancy schemes.
- Considering different techniques for output waveform synthesis.
- Investigating recoverable overcurrent protection.
- Comparing series regulation with the add-on method.
- Considering the elimination of filtering in the regulator section for possible weight reduction.
- Comparing power switching transistors to silicon-controlled rectifiers.
- Checking preferred circuits libraries for improvements in conventional type circuits.
- Reviewing qualified parts lists.

These considerations are aimed at obtaining improved components and techniques for improving both performance and life. So long as significant improvements can be introduced in the equipment design, considerations of the type identified above continue. The major goal of this is to select a complete design that incorporates all desirable features. For the static inverter the logical conclusion of this effort is the initial schematic diagram for the complete circuit with sufficient parts designated to permit construction of a workable breadboard model.

3.0 Design Stage Analyses

The design stage of the equipment development process begins with the drafting of the initial schematic for the complete circuit and initiation of breadboard construction. The design stage analysis problem is--given the circuit schematic, determine the design which will give maximum reliability. The analysis presented herein is directed toward this aim. Because the prime objective is to investigate new analytical methods, certain techniques have been carried to greater detail than normally necessary. This restricts the application of some of the methods.

The particular approach to the analysis is presented in Section 3.1. The functional analysis in Section 3.2 provides background material for the quantitative analysis in Section 3.3. A summary of results is presented in Section 3.4.

3.1 Analysis Method

A previous contract effort (Contract NASw-334) has provided guidance for a methodical approach to reliability. This is described in Vol. I, Section 1.3 of this report. Emphasis is placed on the relation of performance and life to equipment reliability. Any design action intended to increase the likelihood of success for either should also consider the effect on the other to assure that the net result is not a decrease in reliability.

Vol. I identifies and describes techniques for performing such analyses and considers their interrelationship with other design efforts. The inverter analysis presented in the following sections illustrates many of these features by employing selected techniques in resolving specific design problems. The basic approach is modeling - designating performance attributes in order to characterize the operation of the equipment and determining cause and effect relationships between these attributes and the factors that influence their behavior. This allows evaluation of the equipment performance.

In this analysis, the complete inverter package is viewed as an element of a space system and its interaction with other system components during its operation is considered. Of major interest is the influence of the system environment (including the input and load) on inverter life and its ability to perform adequately and conversely the influence of the inverter on the system environment. Since missions have not been designated for the inverter, actual environmental profiles and performance requirements are undefined. Instead, various possible modes of operation in a space system application were considered with purchase specifications for an earlier model inverter as a guide.

From this review of operation and performance requirements, attributes were selected for characterizing the performance for different modes of operation. The analysis was facilitated by functionally decomposing the inverter into lower level elements or smaller circuits.

Analyses of both life and performance were performed. Life considerations were limited to a comparison of different circuit configurations. Failure analyses were used to identify critical modes of component failures, and component stress analyses were used to compare actual stresses to component ratings.

Major emphasis is on performance. This requires the use of conventional engineering models; however, considerable effort was devoted to formulating and using more accurate models than normally employed.

Some of the inverter attributes are directly modeled in terms of attributes of lower level elements and the models used to analyze the design. Typical of this procedure is the analytical model for the output voltage. Some attributes such as transient characteristics and power dissipation are treated empirically using data from the breadboard model. Other attributes, for example RF interference, received less emphasis because of their complexity at this stage of design.

Due to the nature of the circuit, some attributes of lower level circuits are related to inverter attributes only in a discrete manner. For example, the ON level of the timing pulses from the timing section are such that within the complete range of their possible variation there is no effect on the inverter attributes.

Models were used to investigate effects of variations of circuit parameters, inputs and load. Actual statistical distributions of attributes were not obtained nor were probability measures of acceptable performance. The major benefit found in this modeling approach is the information on sources and magnitudes of attribute variability, on the identification of design improvements, and on gaining added assurance for acceptable performance.

Of significant benefit to this study was a complete breadboard model of the circuit. It provided a major source of data as well as serving as a convenient physical model for gaining familiarity with the circuit operation.

3.2 Functional Analysis

The static inverter is designed as a regulated ac power supply for general space system application. Its functional employment as an element of a space system is illustrated in Figure 1. For normal operation, 28 vdc from the system primary power supply is converted into 115 vac, three-phase, 400 cps, sinusoidal power for total loads ranging from 0 to 250 va. Factors which may affect inverter operation include

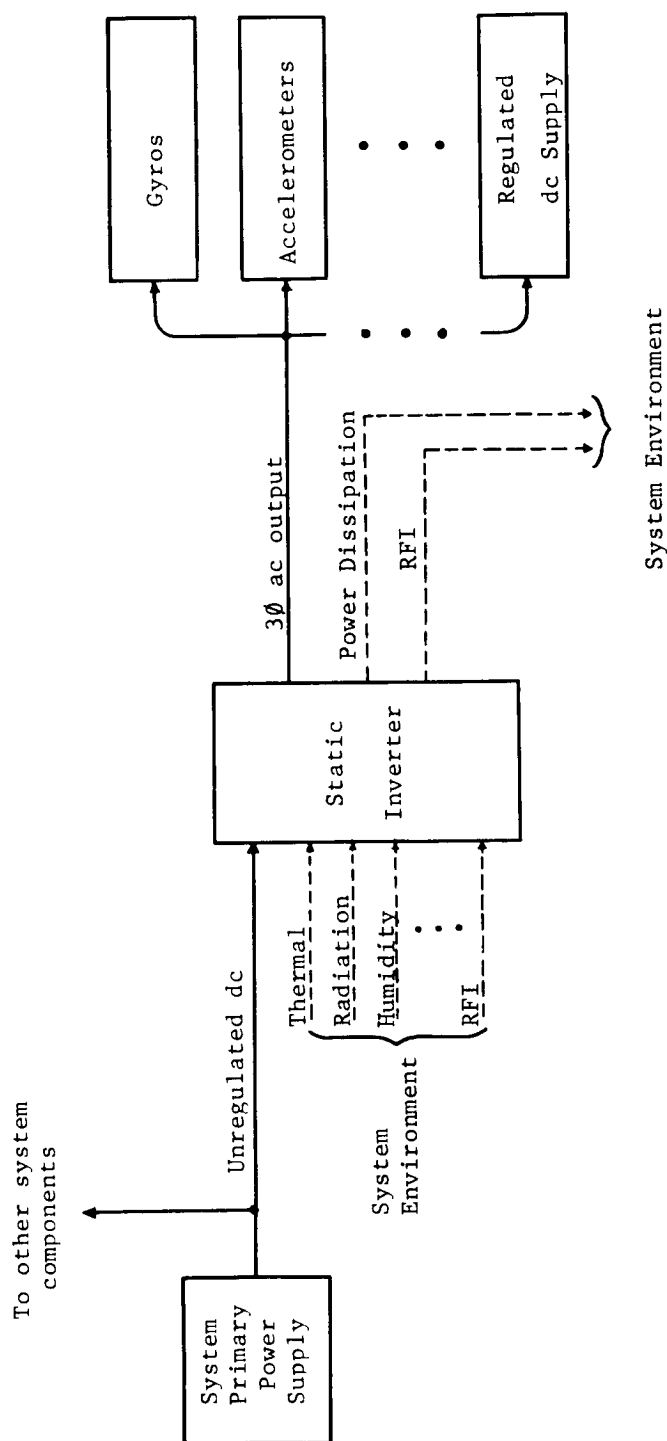


Figure 1. The Static Inverter as an Element of a Space System

(1) variations (both static and transient) of the input dc, (2) load characteristics, and (3) the environment. In turn, effects of the inverter operation on other system components include (1) variations in the three-phase output, (2) influence on other components connected to the input, and (3) contributions to the system environment.

3.2.1 Mission Definition

The inverter is designed as an ac supply for general space system application. This implies as wide a range of operating conditions as is possible. A tabulation of possible mission phases for several space system types and probable operating modes of the inverter is presented in Figure 2. The modes of operation identified are defined below:

(1) Normal Operation

Input power is supplied per load requirements ranging from 0 to 250 va total or 85 va per phase. The inverter output waveform assumes a form which can be adequately described by the joint relations

$$\begin{aligned}e_{AB}(t) &= E_{AB} \cos(2\pi ft + \phi_{AB}) + N_{AB}(t) \\e_{BC}(t) &= E_{BC} \cos(2\pi ft + \phi_{BC}) + N_{BC}(t) \\e_{CA}(t) &= E_{CA} \cos(2\pi ft + \phi_{CA}) + N_{CA}(t)\end{aligned}\tag{1}$$

where

A, B, C are designations for the three-phase inverter output terminals,
e is the instantaneous output voltage,
E is the peak voltage of the fundamental frequency component of the output voltage,
f is the fundamental frequency in cps of the output waveform,
 ϕ is the phase in radians of the fundamental frequency component,
N is the distortion of the output waveform, i.e., the summation of all voltage at frequencies other than the fundamental, and
t is time in seconds.

(2) Turn-on

Input power is applied with the rate of increase determined by the effects of transients on the inverter loads. The inverter is designed to withstand a step change from zero power input to its maximum capability.

(3) Turn-off

Input power is removed instantaneously in all anticipated applications.

System Type	Mission Phases									
	Prelaunch				Flight					
	Manufac- turing	Testing	Storage, Trans., Handling	Prelaunch check	Launch	Orbit	Space Traj.	Re-entry	Landing	Recovery
Launch Vehicle										
Satellite	All Modes		No Operating Modes	All Modes	Modes 1, 4					
Deep Space Probe										
Manned Spacecraft										

Modes: (1) Normal operation
 (2) Turn-on
 (3) Turn-off

(4) Transient response
 (5) Overload
 (6) Load start

Figure 2. Typical Operation Modes of the Static Inverter

(4) Transient Response

This defines brief periods during sustained operation when the output departs from normal in response to disturbances such as input transients and load changes.

(5) Overload

Inverter operation for any load demand greater than 85 va per phase represents the overload mode. Recoverable protection of the inverter circuit during inadvertent overload conditions is provided by the overcurrent protection loop. The threshold for this is nominally at 1.4 amp line current, i.e., 93 va per phase at 115 vac output.

(6) Load Start

This mode describes transient operating conditions occurring when loads requiring significant starting periods (on the order of seconds or minutes) are connected to the inverter output. Short term transients on the order of 0.1 sec or less are included in the transient response mode.

The prelaunch mission phases listed in Figure 2 do not occur in any preselected order and each may consist of more than one stage of operation throughout the pre-launch mission. Most important is the inverter operation at launch which is affected by aging and cumulative stresses throughout the prelaunch period. These include many tests and exposure to many stress conditions which are impractical to specify.

For considering the combined effects of all prelaunch stresses and the acceptability of the inverter at launch, the following is assumed:

Total prelaunch duration = 6 months

Total prelaunch operating time = 720 hours

Prelaunch checkout duration = 2 hours

The inverter has not, to date, been assigned any specific flight missions. The various possible system applications in Figure 2 have similarities; however, environments may differ widely. The earlier generation 450 va inverter is employed only in the Saturn I booster for supplying guidance and control equipment for an approximate five minute flight duration. The present 250 va inverter may find similar application in the Saturn V booster in which strict environmental control is provided. For example, the ambient temperature is maintained near constant at 42°C. Since, however, the inverter may be employed in other systems, the consideration of an extensive range of environments is necessary.

As a basis for performing quantitative analyses, the following is assumed for the flight mission:

Launch phase duration = 15 minutes

Orbit phase = 720 hours

3.2.2 Interface Characteristics

Characteristics of the outputs, inputs, loads, and environmental factors that are of interest in the design analysis are identified below and requirements are considered to the extent feasible. In the absence of specific missions, requirements stated in the specifications for the prior design [Ref. 4] are frequently quoted for guidance. Additional requirements were selected from those for a similar system [Ref. 5] and are assumed to be typical for static inverters. Characteristics for which no specifications are given are also discussed.

Most of the requirements are imposed on the inverter by the system or by other system components (primary dc supply and loads). Examples are output voltage regulation and input voltage requirements.

3.2.2.1 Output

The only output of the inverter is the three-phase ac electrical power. Characteristics of interest for the various operating modes which were defined in the previous section are given below.

(1) Normal Operation Mode

(a) Load voltages: V_{AB} , V_{BC} , V_{CA}

$$V_{AB} = \text{Rms}[e_{AB}(t)]; V_{BC} = \text{Rms}[e_{BC}(t)]; V_{CA} = \text{Rms}[e_{CA}(t)] \quad (2)$$

Nominal: $V_{AB} = V_{BC} = V_{CA} = 115 \text{ vac}$

Requirements: stated below in terms of average three-phase voltage and voltage imbalance.

(b) Average three-phase voltage: V

$$V = \frac{1}{3} [V_{AB} + V_{BC} + V_{CA}] \quad (3)$$

Nominal: $V = 115 \text{ vac}$

Requirements: $\pm 1.0 \text{ vac}$ [Ref. 4]

The inverter allows manual adjustment of V over a minimum range of 110 to 120 vac. This adjustment is made at one half the rated current and 28 vdc input to $115 \pm 0.5 \text{ vac}$. Allowable variations from the preset value over the full range of load and environments are $\pm 1.0 \text{ vac}$. The

breadboard circuitry exhibits an actual adjustment resolution of less than 0.1 vac.

(c) Phase balance voltages: $\Delta V_A, \Delta V_B, \Delta V_C$

$$\Delta V_A = V_{CA} - V_{AB}; \Delta V_B = V_{AB} - V_{BA}; \Delta V_C = V_{BC} - V_{CA} \quad (4)$$

Nominal: $\Delta V_A = \Delta V_B = \Delta V_C = 0$

Requirements: ± 1.5 vac [Ref. 4]

(d) Fundamental frequency: f

Nominal: $f = 400$ cps.

Requirements: ± 0.012 cps. [Ref. 4]

(e) Phase differences: $\Delta \phi_A, \Delta \phi_B, \Delta \phi_C$

$$\Delta \phi_A = \phi_{AB} - \phi_{CA}, \Delta \phi_B = \phi_{BC} - \phi_{AB}, \Delta \phi_C = \phi_{CA} - \phi_{BC} \quad (5)$$

Nominal: $\Delta \phi_A = \Delta \phi_B = \Delta \phi_C = 120$ deg.

Requirements: ± 2.0 deg. [Ref. 5]

(f) Output distortion: D_{AB}, D_{BC}, D_{CA}

Relative distortion of a waveform which is ideally sinusoidal is normally defined as the ratio of the rms voltage of the waveform content at all frequencies other than the desired frequency to the rms voltage of the desired sinusoidal frequency component. Since the distortion of the inverter output consists primarily of harmonics of the fundamental component, the relative distortion is defined by

$$D_{AB} = \frac{\sqrt{\sum_{n=2}^N E_{AB}^2(n)}}{E_{AB}(1)} \quad (6)$$

where $E_{AB}(n)$ is the amplitude of the component at frequency $n \times 400$ cps and N is the total number of components included. Similar definitions also apply to D_{BC} and D_{CA} .

Nominal: 1.7%

This value was computed from the ideal stepped waveform and nominal output filter characteristics. [Appendix, Ref. 1]

Requirements: Less than 5% [Ref. 4]

(g) Output volt-amperes: $(VA)_{AB}$, $(VA)_{BC}$, $(VA)_{CA}$

$(VA)_{AB}$ = load voltage \times load current for phase AB.

Similar definitions apply to phases BC and CA.

Requirements: 0 to 250 va total for the three phases [Ref. 4]; 0 to 85 va per phase implied.

This is the design rating and, as an exception to earlier requirements, represents a requirement imposed by the inverter on the load.

(See Section 3.2.2.3 for load description).

(h) Conducted RFI

Requirements: Defined by MIL 6181-D [Ref. 6] or by an equivalent NASA spec [Ref. 7].

(2) Turn-on Mode

(a) Voltage overshoot: ΔV_i

ΔV_i = Maximum excursion of either phase voltage beyond the steady-state value.

Typical requirement: less than 15% of steady-state voltage [Ref. 5]

(b) Turn-on time: t_i

t_i = time required for all three phase voltages to settle within $\pm 1\%$ of the steady-state value.

Typical requirement: Less than 100 msec. [Ref. 5]

(3) Turn-off Mode

This mode is rarely of interest in application. The major characteristic is turn-off time t_f where

t_f = time required for all three phases to decay to less than 5 vac.

Requirement: Not investigated.

(4) Transient Response

Characteristics of the output during deviations from normal operation are identified below.

(a) Transient amplitude: ΔV_{tr}

ΔV_{tr} = maximum voltage deviation of any phase during a transient.

Typical requirement: $\pm 5\%$ of steady-state value [Ref. 5]

(b) Transient time: t_{tr}

t_{tr} = time required for all voltages to return to within ± 0.1 v. of the steady-state value after a transient.

Typical requirement: Less than 100 msec. [Ref. 5]

(5) Overload Mode

Recoverable overload protection is provided by the overcurrent protection loop. The characteristics of interest are presented below.

(a) Threshold current: I_p

I_p = minimum value of either output line current that causes the overcurrent protection loop to commence operation.

Nominal: 1.4 amps.

Assumed requirements: ± 0.1 amp.

(b) Overload current: I_{OL}

I_{OL} = maximum value of either line current during any overload condition.

Assumed requirement: less than 2 amp.

This allows for operation when the line current demanded is greater than the rated current, but not so as to cause complete shut-down of the inverter operation.

(c) Shut-down time: t_d

t_d = time required for all output line currents to reach their steady-state overload value when the load demands complete shut-down.

Assumed requirements: 100 msec.

The steady-state operation when the load demands shut-down is a limit cycle operation and I_{OL} represents the current as measured by an rms current meter.

(d) Recovery time: t_r

t_r = time required for all output line currents to reach a steady-state value after an overload condition is removed.

Typical requirement: 100 msec. [Ref. 5]

(6) Load Start Mode

Characteristics of interest following application of loads to the inverter are listed below. The effects of short term transients due to sudden application of load are considered under the transient response mode in (4).

(a) Output volt-amperes

Assumed requirements: 280 va maximum for the total of the three phases;
93 va maximum per phase

These requirements are the maximum available output va which is obtained at the output current level required to activate the overcurrent protection loop. During load starting conditions the inverter must be protected against excessive load demands. (See Section 3.2.2.3).

(b) Average three-phase output voltage: V

Requirements: Undefined

If load starting conditions exceed the 250 va capability of the inverter, loss of voltage regulation may result.

3.2.2.2 Input

The unregulated dc is the only functional input to the inverter. During the prelaunch phases, power is supplied by controlled dc rectifier supplies and during flight phases, by storage batteries. The discussion below applies to both type supplies unless otherwise noted.

(1) Normal Operation

Characteristics of the input for normal steady-state operation are defined below.

(a) dc voltage: V_{in}

Nominal: 28 vdc

Requirements: 25 to 30 vdc [Ref 4]

These requirements are imposed by the application for postlaunch operation. Decreasing supply voltages are anticipated due to current drain on the batteries.

(b) Voltage ripple

Requirements: Undefined

This represents quasi-steady state ac ripple components of the input voltage not normally governed by the RFI specification and usually generated within the power sources. Here, it represents the voltage ripple in the source circuit under open circuit conditions. No voltage ripple will result directly from storage battery sources during flight; however, other system elements commonly supplied by the source can induce voltage ripple. This is expected to be small. Voltage ripple from rectifier sources during prelaunch checkout is possible but the amplitude is unknown. The voltage ripple will most likely occur at fixed small amplitudes with the

amplitude changing in small steps as loads are switched on and off the primary dc bus. Due to the large amount of filtering on the inverter input the effect of voltage ripple on inverter performance will be minimal.

(c) Input current: I_{in}

Requirements: Not to exceed 20 amp. at rated load of 250 va [Ref. 4].

The primary contributions to I_{in} are the inverter output load demand, and the inverter internal losses.

(d) Current ripple:

Requirements: Undefined

This refers to the fluctuation in input current caused by the current modulation in the inverter primary voltage regulator. The major factor of interest is the effect of the input current modulation on the source and the other system elements connected to the source. The 9.6 kc voltage ripple is induced at the source terminals and RFI is radiated from the main power bus connecting the source to the inverter.

(2) Turn-on

No requirements are defined for input characteristics at turn-on; however, impedance of the source circuit will effect the current transients as seen by other loads connected to the primary dc bus.

(3) Turn-off

No requirements are defined. Input current may be of interest with regard to switch arcing or the induced transients on other loads connected to the primary dc bus.

(4) Transient Response

With the inverter in steady-state operation disturbances on the input disturb the voltage regulation loop. The most likely input disturbances will be spurious short-duration transients and step changes in load due to switching other loads on and off the primary dc bus. Characteristics of interest are listed below.

(a) Initial voltage

Same requirements as for normal operation.

(b) Voltage step magnitude

Requirements: Undefined

Step changes in input voltage of any magnitude are possible, subject to the constraint that the final voltage is within the requirements of 25 to 30 vdc stated for normal operation.

(c) Spurious transients

Typical requirements:

The inverter shall be capable of withstanding, without damage, input transients as high as 80 v for 0.1 sec. [Ref. 5]. The inverter input filter will attenuate spurious transients thus reducing their effect on the voltage regulation loop.

(5) Overload

The current requirements stated under (1) for normal operation are adequate for this mode.

(6) Load Start

The current requirements stated under (1) for normal operation are adequate for this mode.

3.2.2.3 Loads

The inverter is designed for maximum efficiency when supplying a balanced three-phase load having a delta equivalent of 160Ω per phase with voltage leading load current by 45 deg. Since specific mission assignments have not been made, actual load characteristics are undefined. Loads, in general, can consist of both linear and nonlinear components and may be either single, dual or three-phase. All loads will be designed or modified for compatibility with the nominal 115 vac output voltage. The design requirements stated for other inverter output characteristics will be adequate for most loads encountered.

For inverter design considerations the load is initially assumed, for all modes of inverter operation, to be adequately represented by linear components of resistance, inductance and capacitance in a delta configuration such that the three-phase impedances are described by

$$z_{AB} = R_{AB} + j\omega X_{AB}; z_{BC} = R_{BC} + j\omega X_{BC}; z_{CA} = R_{CA} + j\omega X_{CA} \quad (7)$$

or equivalently

$$z_{AB} = |z_{AB}| e^{j\theta_{AB}}; z_{BC} = |z_{BC}| e^{j\theta_{BC}}; z_{CA} = |z_{CA}| e^{j\theta_{CA}}. \quad (8)$$

Non-linear loads are considered in detail as they are specifically identified.

The major load characteristics are considered for their effect on the inverter design as described below for the different modes.

(1) Normal Operation

(a) Load level

Requirements: Each phase impedance greater than 160 ohms.

This requirement is set by the designed volt-ampere capability of 0 to 250 va total or 85 va per phase.

(b) Power factor

Requirements: Undefined

The basis for requirements on load reactive angles is the inverter efficiency as determined by the magnitude of reactive currents in the main power converter stages at full load.

(c) Load unbalance

Requirements: Undefined

Load unbalance can cause output voltage and phase imbalance but has no significant effect on the ability of the inverter to deliver its rated power. Voltage and phase imbalance requirements stated in Section 3.2.2.1 apply.

(2) Turn-on

The inverter is capable of starting under all load conditions defined for normal operation.

(3) Turn-off

No consideration is necessary.

(4) Transient Response

Instantaneous changes in load can disturb the inverter voltage regulation loop. Load characteristics of interest are listed below.

(a) Initial load level

Same requirements as for normal operation.

(b) Load change

Requirements: Undefined

From the initial load level, step changes of any magnitude are considered possible so long as the overcurrent protection threshold level of 85 va per phase is not exceeded.

(5) Overload

The inverter is designed to protect against all overload conditions including shorts of the output terminals. Requirements on the load for this mode are not necessary.

(6) Load Start

The major load characteristics of interest are the duration of temporary overload conditions during turn-on, i.e., the time required for the load to reach steady-state conditions. Requirements are currently undefined. If starting conditions do not create a temporary overload, requirements are not necessary.

3.2.2.4 Environmental Factors

The extent to which environmental factors are considered during design, and especially during circuit design, is limited by their complexity. Some environmental effects have negligible influence on the functional circuit operation. Others are rendered insignificant by the shielding effect of the system structure or the circuit housing. There are some, however, which are of major concern.

The thermal environment is one of the major influences on both life and performance. Nuclear and cosmic radiation could be important if missions require exposure to high intensities. Mechanical effects such as vibration and acceleration may cause damage or failure.

Several environmental factors important to the inverter are discussed below. Most of the requirements represent environmental test conditions given in the inverter specification [Ref 4]. For brevity and because of sparse information on actual mission environments, these are assumed the same for all modes of operations.

(1) Thermal Environment

These requirements are assumed to include all mission phases and all modes of operation requirements:

- (a) Ambient temperature: -25 to +100 deg. C [Ref. 4]
- (b) Thermal shock: -25 to +125 deg. C [Ref. 4]

The reason for the difference in the upper limits is unknown since, in thermal shock tests, the ambient temperature remains at the upper limit sufficiently long (2 hours) for the inverter operation to stabilize. It is assumed that the -25 to +125 deg C requirement applies to the mission.

The above requirements are assumed to adequately account for all heat transfer mechanisms, convection, conduction and radiation between the equipment and other parts of the system. The limit is set by the maximum operating temperature of the circuit components. The controlling factor on maximum temperature is the junction temperature of the semiconductor devices. The +125 deg C will result in internal "hot spots" of several degrees higher; a maximum hot spot temperature of +135 deg C is considered acceptable.

The inverter supplies heat to thermal environments of other system components through convection, conduction and radiation. The minimum efficiency requirement of 70% for operation at full load allows a maximum dissipation of 110 watts.

(2) Radiation

Requirements: Undefined

The radiation environment is significant only if the inverter is to be used in high radiation flux fields such as the Van Allen belt or in systems employing nuclear power components. Primary characteristics of concern are the types of radiation (gamma, proton, electron, etc.), intensity, and energy levels.

(3) Radiated RF

Requirements: MIL 6181-D [Ref. 6]

The effects of radiated RF interference on the inverter is influenced by the shielding effectiveness of the mechanical package.

(4) Pressure

Requirements: 760 mm Hg (sea level) to 0.17 mm Hg (200,000 ft.) [Ref. 4]

Pressure effects include electrical arcing and less efficient heat transfer. Capability is provided for hermetically sealing the inverter package; however, the necessity depends on whether the system provides a controlled environment. The above requirements represent test conditions for simulating launch phase conditions.

(5) Vibration

Requirements: 20 g rms for 5 minutes [Ref. 4]

The above requirement represents test conditions to simulate the anticipated vibration profile for the launch phase. Anticipated vibration profiles for other phases is less severe.

(6) Acceleration

Requirements: 10 g for 6 minutes in each direction along the three mutually perpendicular axes [Ref. 4]

These test conditions simulate the acceleration profile for the launch phase.

(7) Shock

Requirements: Maximum shocks of 50 g for 6 to 11 ms. duration [Ref. 4]

This test condition is assumed to adequately represent the extreme shock conditions for all phases.

3.2.3 Reliability Considerations for the Inverter Design

From the review of operating modes, missions and interface characteristics for the complete inverter, specific reliability considerations are identified. A summary of performance attributes selected to characterize the inverter operation for all modes is presented in Table I. For use in modeling the attributes (as described in Section 3.1) the factors that influence attribute behavior are also listed. The requirements stated in Section 3.2.2 are employed for adjusting acceptability of operation. However, failure to meet the stated requirements under all conditions will not automatically cause rejection; rather the observed variations coupled with detailed knowledge of circuit operation will provide bases for engineering judgment on performance acceptability.

Four reliability analysis tasks have been performed for the inverter:

(1) component failure modes and effects analysis, (2) performance variation analysis, (3) component stress analysis, and (4) reliability prediction. Their contributions to inverter reliability assurance are described in separate discussions below.

(1) Failure Modes and Effects Analyses

A failure modes and effects analysis considers different modes of operation of components and the effect each has on equipment operation. Failure of a specific component in a particular mode may either result in no significant effect on the equipment, cause degraded performance, or result in complete failure of the system; thus critical modes of failure can be identified, citing the possible need for corrective action.

A failure modes and effects analysis employing three-state logic for components, i.e., normal operation, failed open, and failed short is performed in Section 3.3.1.2 for the inverter circuit. This illustrates the procedures and utility of this type of analysis. For the inverter, it was abbreviated to considering failure modes of components individually and assessing their effects with simple analyses or with engineering judgment. More extensive approaches are possible. Experience has indicated that failure modes and effects analyses are invaluable as guidance in identifying the modes of equipment behavior to be analyzed in other efforts. It is now recognized that in a comprehensive effort the failure modes and effects analysis should be initiated prior to other efforts.

(2) Performance Variation Analyses

Performance variation analyses consider the continuous variation in the performance attributes for various equipment operating modes. For the six modes of operation (normal operation, turn-on, transient response, etc.) identified in

TABLE I

Summary of Inverter Performance Attributes
and Influencing Factors for Operating Modes

Mode	Performance Attribute	Influencing Factors (Exclusive of Environments)
Normal operation	Output frequency	Input voltage
	Average three-phase output voltage	Input voltage ripple
	Output voltage imbalance	Load level
	Output phase imbalance	Load power factor
	Output distortion	Load imbalance
	Input current modulation	Conducted RFI
	Power dissipation	
	RF interference	
Turn-on	Output voltage overshoot	Input voltage
	Turn-on time	Load
Turn-off	Turn-off time	Load
Transient response	Maximum output voltage devi- ation during a transient	Input voltage
	Transient time	Input transients
		Load level
		Load changes
Overload	Threshold current	Load
	Overload current	Input voltage
	Shut-down time	
	Recovery time	
Load start	Average three-phase output voltage	Load
		Input voltage

Section 3.2.1, performance attributes were identified for each with emphasis on those related to the normal operating and to the transient response modes. The quantitative treatment of the inverter attributes is given in Section 3.3.1.4. Specific attributes designated for lower level elements are treated in other appropriate parts of Section 3.

Other modes of inverter behavior resulting from failed components are recognized and performance variation analyses are of interest for some of these. Typically, the failure of one of the six identical timing channel circuits can lead to degraded (but possibly not totally unacceptable) operation. This mode is also considered in Section 3.3.1.4. A more comprehensive analysis could include more of these.

The techniques employed conform to the modeling approach, either analytical or empirical, as described in Section 3.1. Circuit analyses form the basis for analytical models and the breadboard circuit for empirical models.

The NET-I network analysis program was employed for analysis of one circuit, the clock pulse amplifier, primarily to determine its potential benefit for analyses of this type. The transient response of the circuit was obtained for a full switching cycle and served to verify that switching transients for all circuits of the inverter were insignificant at the relatively low switching frequencies involved. The use of the program for performing steady-state analyses was also investigated, but because of inconvenience it was not employed extensively. The utility of such programs (NET-I, ECAP, etc.) is limited by the cost, data inputs, and the many simplifying assumptions required for their implementation; however, when used with discretion they can be a definite asset in performance variation analyses.

(3) Component Stress Analyses

Component stress analyses are presented in Section 3.3.1.3. These conform primarily to the stress vs. strength concept whereby the major stresses on each component are computed and compared to its strength (or rated conditions in this case). This was used to investigate and illustrate the procedures and was abbreviated to the extent of employing simple models for performing worst-case type computations of electrical stress conditions and making liberal use of assumptions in the absence of data. More extensive analyses are frequently performed but require more sophisticated models. One example is the use of network analysis programs for computing stresses for each component. Sophistication in thermal analyses is being employed, now, to compute realistic thermal stresses. Computed stresses are used in reliability prediction calculations, for refining failure rate estimates, and for relating component variability to stress conditions in performance variation analyses.

(4) Reliability Prediction

Conventional reliability predictions are performed in Section 3.3.1.1 using the following assumptions:

- (a) failures of components are independent,
- (b) components have constant hazard functions,
- (c) the environment is constant,
- (d) failure of a component represents failure in any mode, i.e., two-state models only are employed,
- (e) failure of a component results in circuit failure unless protected by redundancy.

Because of these assumptions, the result is not representative of the actual probability of successful operation of the inverter. The prediction is used solely for comparing different circuit configurations.

In Vol. I of this report, limitations on the utility of this type of analysis are recognized. The over-simplified models employed assume the equipment to be either "alive" or "dead" which excludes drift or performance variation. Some failure rates include "out-of-tolerance" events as failures to account for drift or performance degradation effects; however, this practice is not standard and distinction is rarely provided for identifying such parts. The results of predictions, when considered with results from other efforts are beneficial.

3.2.4 Functional Breakdown for Analysis

The analysis in the following section is facilitated by subdividing the inverter into functional parts. The total breakdown of the complete inverter package into lower level elements down to individual circuit components is summarized in Table II with a numerical designation assigned to each element. With minimal exception, the breakdown is along hardware lines with elements designated at different levels of complexity for performing analyses. The designations containing M denote elements which were modified during the analysis.

Functional diagrams of the inverter circuit showing the interrelationship of the various elements was presented in a previous report [Ref. 1]. A revised functional diagram containing all modified elements is presented in Figure 3. The analyses consider both versions of modified elements; however, the single diagram in Figure 3 is adequate for referring to functional operation.

All elements from the complete inverter circuit level (element 6) down to the small circuit level (element 21 - 64) are identified in Figure 3 with the exception

TABLE II
Equipment Functional Breakdown

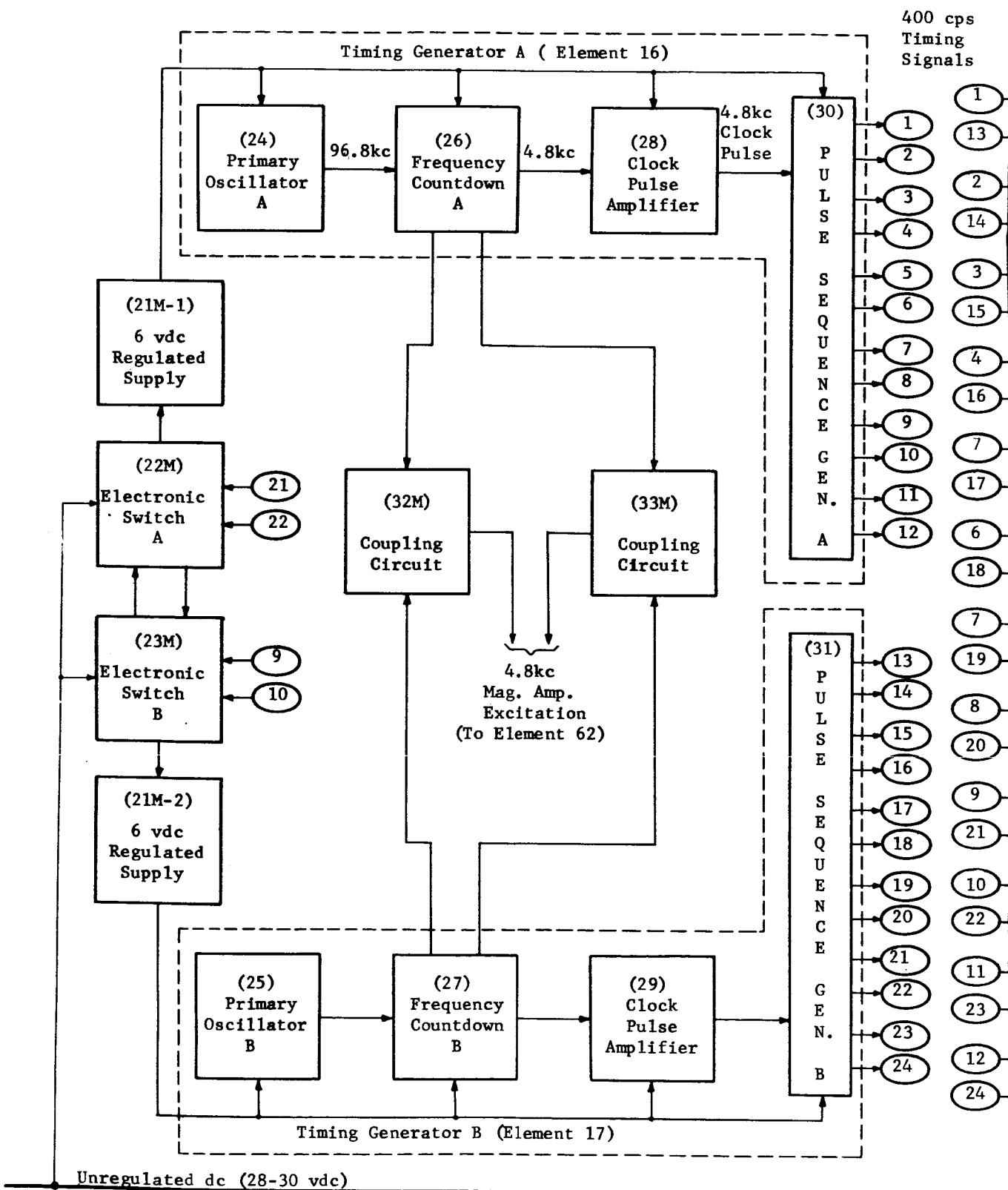
<u>Element No.</u>	<u>Designation</u>	<u>Location</u>
<u>System Components</u>		
1	Static Inverter (Complete Package)	System
2	System Primary Power Supply	System
3	Inverter Load	System
4,5	(Not Used)	--
<u>Major Inverter Parts</u>		
6	Inverter Circuitry	1
7	Inverter Housing	1
8 - 10	(Not Used)	--
<u>Circuit Sections</u>		
11	Timing Section	6
12	Control and Conversion Section	6
13 - 15	(Not Used)	--
<u>Major Circuits</u>		
16	Timing Generator A	11
17	Timing Generator B	11
18	Voltage Regulation Loop	12
19	Overcurrent Protection Loop	12
20	(Not Used)	--
<u>Small Circuits</u>		
21	Six-volt dc Regulated Supply (Original Version)	11
21M-1	Six-volt dc Regulated Supply A (Modified Version)	11, 16
21M-2	Six-volt dc Regulated Supply B (Modified Version)	11, 17
22	Electronic Switch A (Original Version)	11, 16
22M	Electronic Switch A (Modified Version)	11, 16
23	Electronic Switch B (Original Version)	11, 17
23M	Electronic Switch B (Modified Version)	11, 17
24	Primary Oscillator A	11, 16
25	Primary Oscillator B	11, 17

TABLE II (continued)

<u>Element No.</u>	<u>Designation</u>	<u>Location</u>
<u>Small Circuits (continued)</u>		
26	Frequency Countdown Circuit A	11, 16
27	Frequency Countdown Circuit B	11, 17
28	Clock Pulse Amplifier A	11, 16
29	Clock Pulse Amplifier B	11, 17
30	Pulse Sequence Generator A	11, 16
31	Pulse Sequence Generator B	11, 17
32, 33	Coupling Circuits 1 and 2 (Original Version)	11
32M, 33M	Coupling Circuits 1 and 2 (Modified Version)	11
34 - 45	Coupling Circuits 3 - 14 (Original Version)	11
34M - 45M	Coupling Circuits 3 - 14 (Modified Version)	11
46 - 51	Timing Pulse Amplifier 1 - 6 (Original Version)	11
46M - 51M	Timing Pulse Amplifier 1 - 6 (Modified Version)	11
52 - 57	Power Converters 1 - 6	12, 18, 19
58	Output Circuit	12, 18, 19
59	Voltage Error Detection Circuit	12, 18
60	Overcurrent Detection Circuit	12, 19
61	20-Volt dc Regulated Supply	12
62	Magnetic Amplifier Driver Circuit (Original Version)	12
62M	Magnetic Amplifier Driver Circuit (Modified Version)	12
63	Magnetic Amplifier	12, 18, 19
64	Primary Voltage Regulator	12, 18, 19

Circuit Parts

The next level of breakdown is in terms of individual components. A complete parts list is presented in Appendix F.



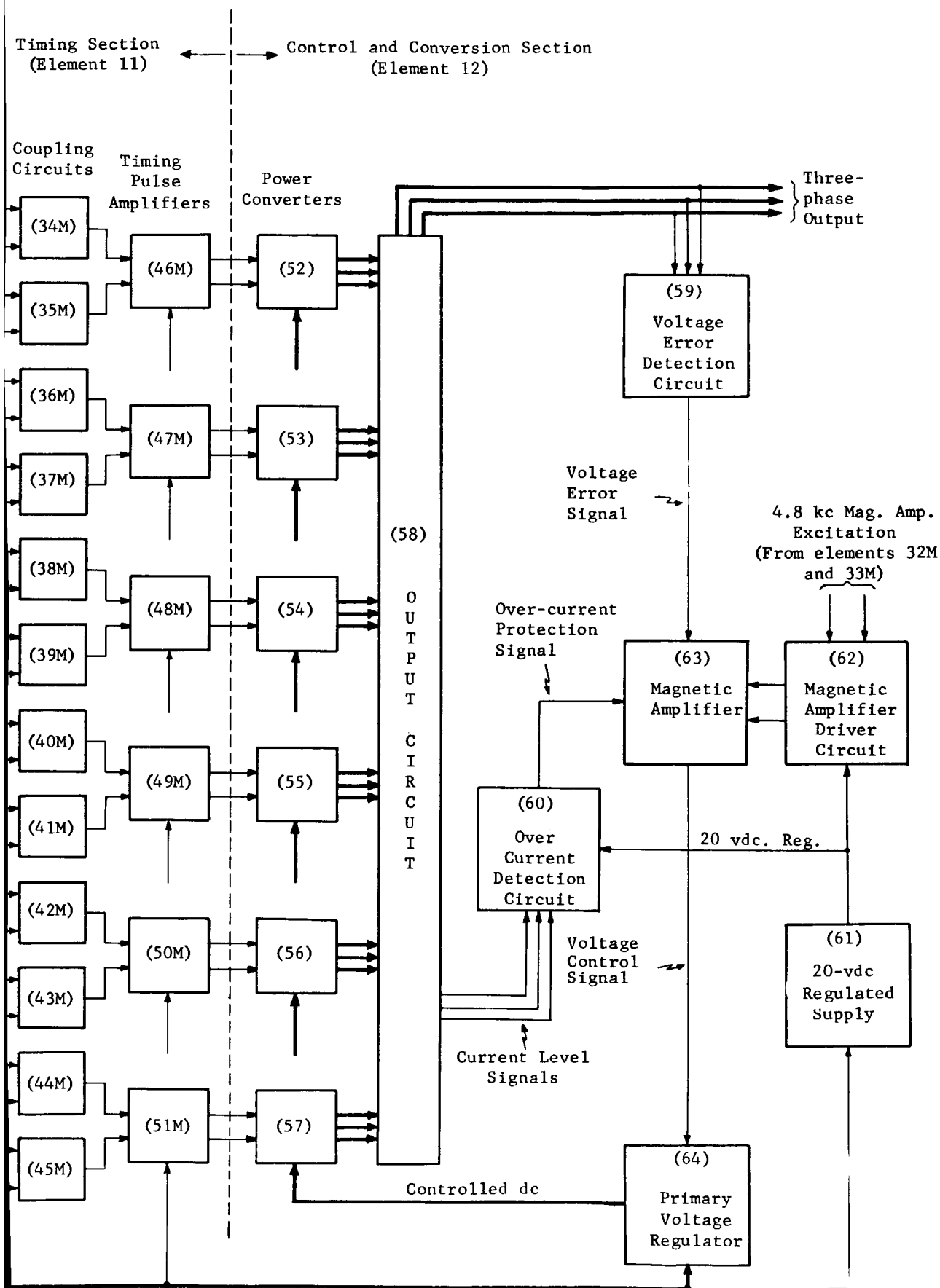


Figure 3. Functional Diagram of the Static Inverter

of element 18, the voltage regulation loop, and element 19, the overcurrent protection loop. These are introduced later as special functional elements for performing specific analyses.

3.3 Quantitative Analyses

The quantitative analyses for the circuit design stage are presented in this section starting with the inverter circuitry and following the functional pattern presented in the previous section.

When analyses are of the type conventionally performed in design, emphasis is on results. Conversely, when the analyses extend beyond conventional types, more detail is presented.

3.3.1 Analyses for the Complete Circuit (Element 6)

Four major areas of analysis for the inverter were identified in Section 3.2.3. Of these, reliability prediction, failure modes and effects analyses, and component stress analyses on individual component behavior are best carried out irrespective of the intermediate levels of circuit breakdown. These are discussed in the following paragraphs.

3.3.1.1 Reliability Prediction

This analysis considers simple computations of success probabilities for the inverter circuit assuming exponential life distributions for components for comparing different circuit configurations. The assumptions inherent in this analysis are listed in Section 3.2.3, and because of these, the results do not adequately represent the predicted reliability of the inverter.

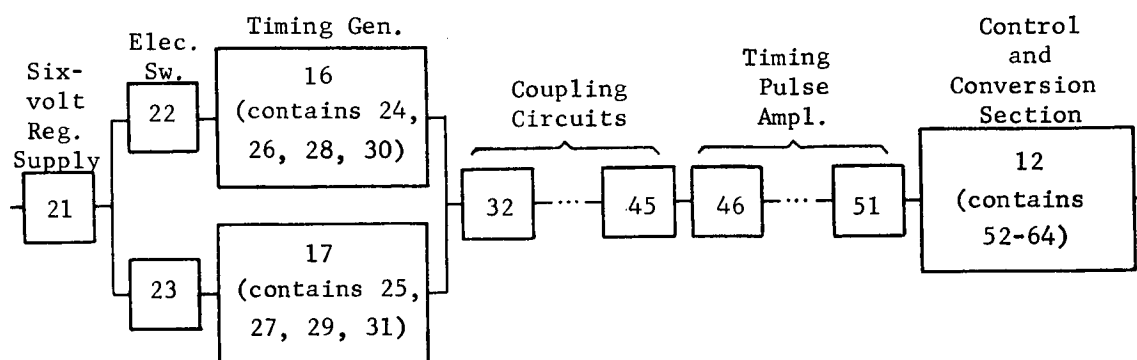
Reliability prediction calculations require specifying a mission, and for the analysis performed an assumed mission is defined as follows:

Stage 1 (all prelaunch operating phases)	- 720 hrs.
Stage 2 (launch)	- 15 min.
Stage 3 (orbit)	- 720 hrs.

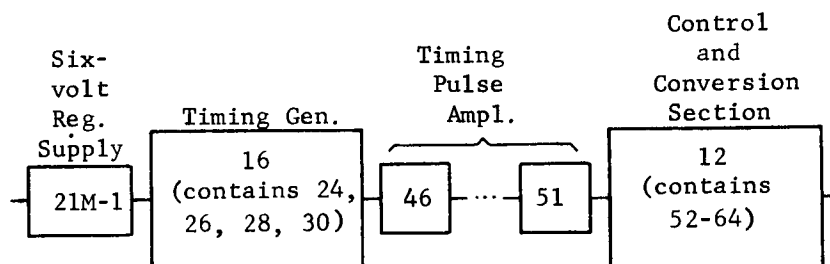
The three configurations of the circuit considered in the analysis are described below and the basic logic diagrams for each are presented in Figure 4.

(1) Original Version (with redundancy)

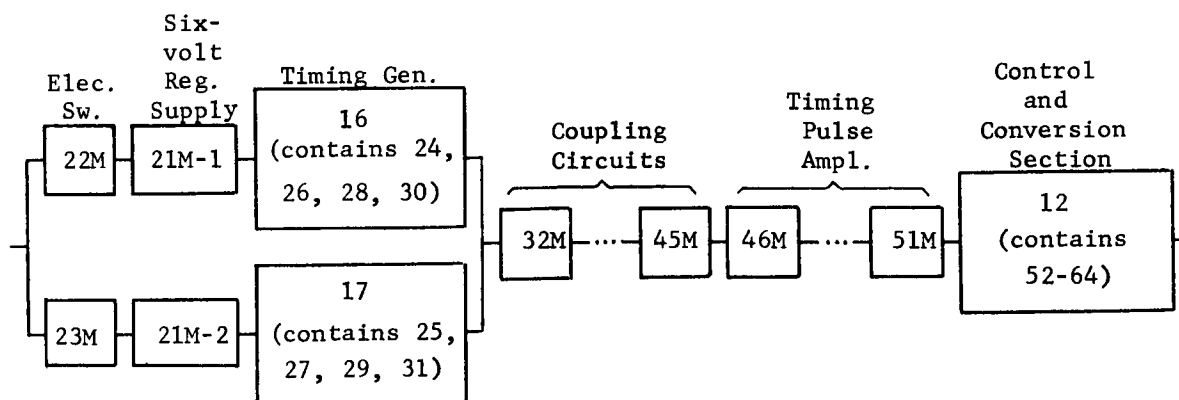
The two timing generator circuits operate in standby redundancy as controlled by the electronic switches. The six-volt regulated supply has internal standby



Original Version (with redundancy)



Original Version (without redundancy)



Modified Version (with redundancy)

Figure 4. Inverter Logic Diagrams for Reliability Prediction

redundancy (described in Section 3.3.4.1). Active redundancy formed by diode quads is provided in the coupling circuits (elements 34 - 51 only) (described in Section 3.3.4.7).

(2) Original Version (without redundancy)

All redundancy in the circuit is eliminated. This eliminates the electronic switches and the coupling circuits. The six-volt regulated supply is simplified to a circuit equivalent to the modified version in Section 3.3.4.1.

(3) Modified Version (with redundancy)

All modified elements are employed including the resistive coupling recommended [Ref. 3] over the diode coupling. The logic configuration is revised to include simpler six-volt regulated supplies in the separate redundant paths with the timing generators. The modified electronic switches switch the unregulated dc input instead of the regulated 6 vdc as in the original version.

Computations are described in Vol. I, Section 4.2.1.2. For specifying part application factors, 30°C for ambient temperature and 50% of rated stress were assumed. No allowance was made for the failures due to poor workmanship during assembly.

Results are presented in Table III for the three circuit configurations. To formulate the event probabilities, let S_j represent the event of success (no failure) for stage j . $P(S_1)$ thus represents the probability of no failure through stage 1. The probability of no failure through stage 2 is

$$P(S_2 S_1) = P(S_2 | S_1) P(S_1), \quad (9)$$

and through stage 3,

$$\begin{aligned} P(S_3 S_2 S_1) &= P(S_3 S_2 | S_1) P(S_1) \\ &= P(S_3 | S_2 S_1) P(S_2 | S_1) P(S_1). \end{aligned} \quad (10)$$

Each conditional event probability tabulated thus represents the probability that the inverter is operating successfully at the end of a particular stage given that it was operating successfully at the start of the period of interest.

The probability, $P(S_3 S_2 | S_1)$, is the most important result. It states the probability of mission success given that the system was operating successfully at launch and is analogous to the reliability for the flight phases only. From equation (10)

$$P(S_3 S_2 | S_1) = P(S_3 | S_2 S_1) P(S_2 | S_1), \quad (11)$$

TABLE III

Summary of Reliability Prediction Calculations

Stage	Event* Probability	Predicted Success Probability		
		Original Version (With Redundancy)	Original Version (Without Redundancy)	Modified Version (With Some Redundancy)
1	$P(S_1)$	0.999988	0.999987	0.999987
2	$P(S_2 S_1)$	0.9965	0.9963	0.9964
3	$P(S_3 S_2 S_1)$	0.9900	0.9894	0.9897
2 and 3	$P(S_3 S_2 S_1)$	0.9865	0.9857	0.9861

* S_j = event of success for stage j

i.e., the product of the individual probabilities computed for stages 2 and 3. Differences among the probabilities for the three circuit configurations appear only in the fourth significant figure, which is insufficient to allow any firm conclusions. Slight improvement in the original version is indicated with the use of redundancy, but from the calculations it is obvious that the improvement in the logic provided by redundancy is offset by the additional parts required for the electronic switches and coupling circuits. Later sections support the use of redundancy in the timing generators on the basis of uncertainties in the performance of the integrated circuits. Because of components sizes, there is little change in overall weight or volume.

Consideration of the efficiency of the six-volt regulated supply and the failure modes of components in both the six-volt regulated supply and the coupling circuits led to the modified version as a candidate configuration. The predicted success probability for the flight stages reflects a small decrease from that of the original

version. However, as discussed below, both performance and failure probabilities definitely favor use of the modified configuration. The change in calculated success probability due to the six-volt regulated supply modification is insignificant, affecting at most the sixth significant figure. In the electronic switch modification, similar parts having the same failure rates were used and thus did not affect the results. A major change resulted from modifications in elements 32 - 51 and 62 in the redesign of the coupling circuits. An investigation was performed and reported [Ref 3] and it was shown in that report that the use of two-state logic (success and failure) for components led to erroneous results. A more thorough study of component failure modes and effects and circuit performance resulted in the selection of the modified version as the preferred configuration.

The trends in the above comparisons are reflected in the computed probabilities for the individual stages. As shown in the analysis in Vol. I, the probabilities are influenced by the environmental factors which characterize the particular stage and are used to adjust the expected number of failures. For example, environmental factors of 900 and 0.9 were used for stages 2 and 3 respectively. Even though the duration of stage 2 is only about 1/3000 that of stage 3, the expected number of failures is about 1/3.

Because of the ability to repair and maintain the inverter during prelaunch phases, a preferred measure of success is the expected number of failures. Using an environmental factor of 0.001, the computed values were 12.5, 13.2, and 12.9 failures per 10^6 hours for the three configurations in the order presented, or about 0.01 failures on the average for the total 720 hours of operation. This figure is probably low but is due to the environmental factor used which is commonly employed in practice. An average of one failure per the 720 hr. duration is a more reasonable estimate.

The small differences in predicted success probabilities, the assumptions required, and the precision of the data preclude their use in determining the preferred circuit configuration. Neither do the results adequately represent the reliability of the circuit. This illustrates the limitations of this procedure. It does provide a more detailed understanding of functional operation and when the results are combined with other major design efforts, contributes to reliability assurance.

3.3.1.2 Failure Modes and Effects Analysis

Failure modes and effects analysis considers the different modes of failure of components and their effect on equipment operation. A major benefit is the identification of critical modes that cause complete failure of the equipment and

marginal modes that result in degraded operation. This, in turn, identifies corrective actions for improving the design. An additional benefit is the identification of failure events to include in reliability prediction calculations.

This analysis is not comprehensive; however, it adequately illustrates the technique and provides informative results about the inverter design. Component failures (and their modes) are considered independently, while all other components are assumed to be operating normally. Thus, if a particular component failure mode is eliminated by redundancy, the mode is not critical and the joint occurrence of the failure modes of redundant components is not included. (An exception is where combinations of failure modes for redundant diodes was considered for comparing circuit configurations [Ref. 3].)

A summary of the failure modes of all circuit components and their effects on circuit operation is presented in Appendix C. The component failure modes considered are "open" and "short". Effects are identified for the immediate circuitry and for the overall inverter operation. Many effects are obvious; some are supported by analysis and discussion in later sections; other are selected on the basis of subjective criteria. Recommendations for corrective actions, when considered, are presented in later sections.

The major criteria used in identifying failure modes and effects are as follows:

(1) Open

For two terminal devices "open" implies either the device itself or its connecting leads open circuit. This also applies to the three terminal pairs for transistors and potentiometers. For other devices such as transformers and flip-flops having more than three terminals, "open" implies loss of connection or open circuit for the particular lead considered. This reflects the effects of extreme changes in device characteristics that tend to make it appear as an open circuit, as for example a diode forward drop becoming very large.

(2) Short

For two terminal devices and terminal pairs for transistors, "short" implies a shunt either within or around the device. For other devices such as transformers and flip-flops, "short" implies a shunt around the device between the specific pairs of terminals considered. This mode also reflects the extreme changes in device characteristics, as for example a diode forward drop becoming very small for large currents.

(3) Failure

Failure is assumed to occur if the circuit or inverter fails to perform a function of any utility. For example, failure of the inverter to conform to its speci-

fications does not necessarily imply a failure since the output, even though degraded, may still be useful for some applications. In certain cases, failure is designated conditional when it depends on the normal state of other components, as for example whether a particular switching transistor is ON or OFF. For some situations failure is delayed when an overstressed condition on one component caused by failure of another component requires a significant time before failure occurs. Some failures are indicated as possible failures when the effects depend on accompanying effects on other components, for example, whether a transistor collector-to emitter fails in a shorted or open mode.

(4) Degraded Performance

This identifies operation that has some functional utility but is not normal, as for example, degradation of voltage regulation.

(5) Degraded Output

This identifies a specific type of degraded performance for the entire inverter wherein the output does not conform to specifications. It may still be useful for some application.

(6) Sustained Operation

This represents the condition when the functional operation continues without significant departure from nominal operation.

3.3.1.3 Component Stress Analyses

Stress analyses in which the ratings of every component are compared with the actual stress conditions are essential to a reliability analysis of an equipment. The static inverter components have been analyzed for stresses and the results of these analyses are summarized in tabular form in Appendix E. Only electrical stresses, i.e., power dissipations, voltages and currents, are considered. Radiation and mechanical stresses that are likely to be encountered, for example, are unknown and component capabilities with respect to these stresses are not specified. The thermal environment is accounted for by derating each component in accordance with manufacturer's instructions such that its specified ratings are known at the extreme limits of the environment.

Reference 2 includes analyses similar to the stress analyses presented herein. The results of the analyses presented in this report are more accurate principally because more and better component data were available. The improved data includes both manufacturer specifications and screening specifications used by the cognizant design group to assure certain parameter value limits. These data provided for improved end-limit or worst-case parameter estimates, and for improved estimates of

component ratings at other than nominal conditions. In Reference 2, nominal or measured component parameters were frequently used because of insufficient component characteristic data. Worst-case estimates of transistor power dissipations are calculated from available data in preference to the rule-of-thumb estimates used in Reference 2. In general, improved component data, system specifications, more informed assumptions and increased precision in calculations have provided for more accuracy in these later analyses.

Liberal use is made of "is less than" and "is greater than" statements in the stress analysis tables of Appendix E. If it can be quickly ascertained that a resistor, for example, is rated at 3.5 watts at 150°C, since the maximum temperature of interest here is 125°C, Table E-1 in Appendix E may state only that the 125°C power dissipation rating "is greater than" ($>$) 3.4 watts. Also, if it can be quickly ascertained that the maximum required power dissipation of the resistor "is less than" ($<$) 0.35 watts, for example, this statement is also entered into the table since more precise estimates are of negligible interest.

No reference is made in Appendix E to stress analyses for transformers, inductors or the magnetic amplifier. For all of these, it has been ascertained that the maximum current densities in the windings are satisfactory. It has also been ascertained both by computation and experimental observations that the transformer cores will not saturate. For the inductors, it has been ascertained that the cores have adequate volt-second capacities and that they operate in an approximately linear region. It was reported that L5 had been observed to "bottom", i.e., operate in the lower half of its B-H characteristics, with zero external load, but the resulting transients were small [Ref. 2]. For this particular application, it is desirable that L5 operate only in the upper half of its B-H characteristics. In order for H to become negative, current must flow through L5 in the direction of Q19-Q21, R71 and CR151 and high transient voltages could result.

Estimates of worst-case power dissipations, voltages and currents were made using worst-case purchase tolerances for parameter values and worst-case values for variables.

The individual stress analysis tables are discussed in Appendix E.

3.3.1.4 Performance Variation Analyses

Analysis of performance variations with the inverter attributes are presented below.

(1) Normal Operation Mode

(a) Output Frequency

Due to the method of generating the output waveform [Ref. 1], the output frequency and its stability are related directly to the operation of the primary oscillator circuits. The nominal 400 cps output frequency is derived from the primary oscillator nominal frequency of 76.8 kc, a reduction of 192. The ± 0.012 cps stability requirement on the output frequency is similarly translated to ± 2.3 cps for the stability of the primary oscillator. Further considerations are presented in Section 3.3.4.3.

(b) Average Three-phase Output Voltage

This is directly dependent on the operation of the voltage regulation loop and the analysis is presented in Section 3.3.3.2.

(c) Output Voltage Imbalance

The major contributions to imbalance in the output voltage are imbalance in load and variations in output circuit part characteristics. A summary discussion of the output circuit is presented in Section 3.3.4.10; however, performance variation analyses of the output voltage imbalance are given below. Output phase imbalance is jointly considered here since the circuit relationships for this attribute are closely related to those for voltage imbalance.

An analytical modeling approach was selected to investigate the behavior of these attributes. Circuit equations are presented in Appendix A for the simplified version of the output circuit shown in Figure A-1. These equations were used to compute voltage and phase imbalance due to variations in circuit parameters. To limit the number of computations, only the fundamental 400 cps frequency component was used. For the specified maximum 5% distortion, it was established that the per cent error in output voltage resulting from neglecting the harmonics is less than 0.125%.

Voltage imbalance is defined explicitly by voltages ΔV_A , ΔV_B and ΔV_C in equations (A-39) - (A-41) with requirements of ± 1.5 v minimum variation. Phase imbalance is similarly defined by angles $\Delta \phi_A$, $\Delta \phi_B$, $\Delta \phi_C$ in equations (A-42) - (A-44). These angles are nominally 120 deg. with assigned requirements of ± 2.0 deg. variation.

In Figure A-1, the ideal voltage sources V'_{ab} , V'_{bc} , and V'_{ca} and the resistances r_{ab} , r_{bc} , and r_{ca} represent the three-phase interconnection of the secondary windings of the output transformers. Impedances z_{AB} , z_{BC} , and z_{CA} represent the inverter load. The voltage error and overcurrent

detection circuits provide negligible loads [Ref. 2], and similarly the primary windings of the current sensing transformers have negligible impedance; therefore, these were neglected for the analysis.

Table IV presents the values of circuit parameters used in the analysis. The variations of the L's, C's, and r's were chosen to represent maximum possible variation. Various values of load impedance magnitudes and reactive angles as listed were investigated (+ angles represent inductive loads.) The source voltages were kept balanced during all computations since the variations of part characteristics within the source circuitry (i.e. the power converters) produce negligible imbalance.

Voltage and phase imbalances resulting from individual variations in part characteristics are summarized in Table V for the three levels of balanced resistive loads. Because of circuit symmetry, it is necessary to specify only one each of the three voltage and phase differences. The individual variations of ΔV_A and $\Delta \phi_A$ do not exceed the requirements. maximum variations of both are caused by variations in L_2 ; and 1.26 v for ΔV_A and 0.69 deg. for $\Delta \phi_A$ at full load. Effects of resistance variations are small and the trends with decreasing load (i.e., increasing load impedance) are acceptable. Effects of inductance variations improve with decreasing load while there is a slight degradation of the effects of capacitance variations as load decreases.

TABLE IV
Output Circuit Parameter Values

<u>Circuit Parameter</u>	<u>Nominal Value</u>	<u>Variation</u>
L_1, L_2, L_3	1.67 mh	± 0.33 mh
C_1, C_2, C_3	2.0 μ f	± 0.4 μ f
r_{ab}, r_{bc}, r_{ca}	5.0 Ω	$\pm 1.0\Omega$
Z_{AB}, Z_{BC}, Z_{CA}	--	160, 360, 1600 Ω
$\theta_{AB}, \theta_{BC}, \theta_{CA}$	--	0, +45 deg.
$V'_{ab}, V'_{bc}, V'_{ca}$	115 vac	--
$\omega/2\pi$	400 cps	--

TABLE V

Variations of Output Voltage and Phase for
Variations in Output Circuit Parameters (Balanced Resistive Load)

Parameter	Voltage Imbalance ΔV_A			Phase Imbalance $\Delta \phi_A - 120 \text{ deg.}$		
	Load Condition			Load Condition		
	160 Ω (volts)	320 Ω (volts)	1600 Ω (volts)	160 Ω (deg.)	320 Ω (deg.)	1600 Ω (deg.)
r_{ab}	0.71	0.37	0.07	0.26	0.28	0.29
r_{bc}	0.08	0.06	0.05	-0.02	-0.01	0
r_{ca}	-0.78	-0.43	-0.12	-0.25	-0.27	-0.28
L_1	1.20	0.63	0.14	0.37	0.42	0.44
L_2	-1.26	-1.08	-0.90	0.31	0.05	-0.28
L_3	0.07	0.45	0.75	-0.69	-0.47	-0.16
C_1	-0.71	-0.77	-0.82	0.52	0.52	0.52
C_2	-0.04	-0.01	-0.01	-0.42	-0.43	-0.45
C_3	0.76	-0.78	0.81	-0.11	-0.09	-0.08

Effects of reactive loads were investigated by computing similar variations in ΔV_A and $\Delta \phi_A$ for reactive angles θ_{AB} , θ_{BC} , and θ_{CA} equal to +45 deg. representing an inductive-resistive series load. The effect is summarized in Table VI which also contains values obtained for balanced resistive load conditions to permit direct comparison. Variations of transformer secondary winding resistances are omitted since they were shown in Table V to be least severe. Only minor differences for capacitance are evident. For inductance, the trends with changing load are different for the two load angles; however, the resistive load still provides the greatest variation. Similar results for $\Delta \phi_A$ were obtained but, for sake of brevity, are not tabulated since they revealed much less variation in comparison to requirements.

Effects of unbalance in load on voltage and phase imbalance were investigated separately by computing variations in ΔV_A and $\Delta \phi_A$ for all possible

TABLE VI

Effect of Load Reactive Angle on Voltage
Imbalance (Balanced Load)

Parameter	Load Angle (deg.)	Voltage Imbalance, ΔV_A		
		<u>Load</u>		
		160 Ω (volts)	320 Ω (volts)	1600 Ω (volts)
L_1	0	1.20	0.63	0.14
	+45	0.69	0.40	0.10
L_2	0	-1.26	-1.08	-0.90
	+45	0.08	-0.61	-0.79
L_3	0	0.07	0.45	0.75
	+45	-0.78	0.21	0.69
C_1	0	-0.71	-0.77	-0.82
	+45	-0.70	-0.76	-0.82
C_2	0	-0.04	-0.01	-0.01
	+45	0.01	0.01	0.02
C_3	0	0.76	0.78	0.81
	+45	0.69	0.74	0.79

combinations of the three load levels considered. This represents extreme unbalanced load conditions for the inverter but adequately serves to reveal the effect of load unbalance. A summary of the results is presented in Table VII. Because of circuit symmetry only seven combinations are required. The greatest imbalance in both voltage and phase occur when two of the phase loads are 160 ohms and the other is 1600 ohms, giving 6.2 v

TABLE VII

Effects of Load Imbalance
on Voltage and Phase Imbalance

Load Combinations			Voltage Imbalance			Phase Imbalance		
Phase AB	Phase BC	Phase CA	ΔV_A (volts)	ΔV_B (volts)	ΔV_C (volts)	$\Delta \phi_A$ (deg.)	$\Delta \phi_B$ (deg.)	$\Delta \phi_C$ (deg.)
320	160	160	-3.42	0.67	2.75	-1.10	1.14	-0.04
1600	160	160	-6.20	1.19	5.02	-2.03	2.07	-0.04
320	320	160	-0.60	-2.78	3.39	-1.14	0.04	1.10
1600	320	320	-2.76	0.46	2.30	-0.93	0.92	0.01
1600	1600	160	-0.95	-5.15	6.11	-2.07	0.04	2.03
1600	1600	320	-0.42	-2.34	2.75	-0.92	-0.01	0.93
1600	320	160	-3.33	-2.32	5.64	-2.07	0.96	1.11

for ΔV_A and 2.07 deg. for $\Delta \phi_A$. Phase imbalance is only slightly greater than the assumed ± 2.0 deg. requirement. Voltage is approximately four times greater than the stated requirements of ± 1.5 v; however, the result is not alarming since the unbalance in load is probably much greater than will ever be encountered in the inverter application. Time did not permit further investigation to determine the extreme load imbalance conditions that are compatible with requirements. This could be accomplished by computing voltage variations for various combinations of load levels that are more equal.

These results reflect primarily the individual effects of the circuit parameter variations on voltage and phase imbalance. Interaction among the phase load levels are included by considering load imbalance. Due to the enormous computation requirements, specific interaction effects of other parameters were not investigated. To include interaction effects a limited number of computations were performed for various combinations of parameter values and worst-case imbalance results selected from these. Balanced full load conditions for reactive angles of 0 and plus 45 deg. were used. As a criterion for selecting the combinations of variations, sixteen runs were employed which is the smallest number that would make

possible uncorrelated estimates of the linear effects of the variables. The greatest imbalance observed in voltage and phase was 5.6 v and 2.54 deg. respectively. These values are strongly dependent on the circuit parameter variations listed in Table IV. These parameter variations purposely represent overestimates.

The results verify that the phase imbalance requirement of ± 2.0 deg. is achieved without difficulty. The maximum voltage imbalance is approximately four times the ± 1.5 v requirement. Again, the analysis could be refined if improved estimates of circuit parameter variations were available. In a final estimate of load unbalance extremes which provide compatibility with voltage imbalance requirements, the collective effect of all variations of circuit part characteristics should be included.

(d) Output Phase Imbalance

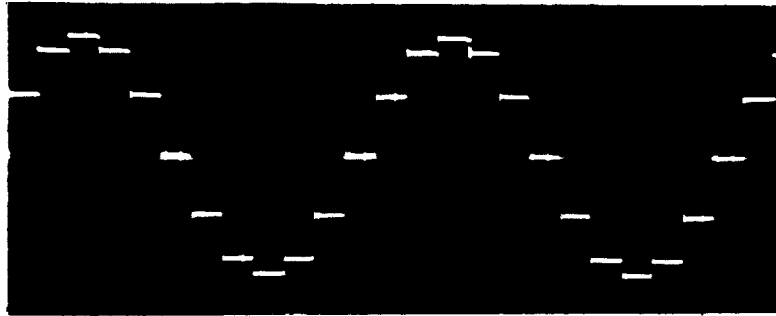
This attribute was analyzed jointly with voltage imbalance above and on the basis of that analysis it is concluded that the typical requirements of ± 2.0 deg. are adequately met. Possible phase imbalance is small due to the inherent manner of generating the output waveform and contributions result only from load unbalance and variations in output circuit parameters which are more critical to voltage imbalance.

(e) Output Distortion

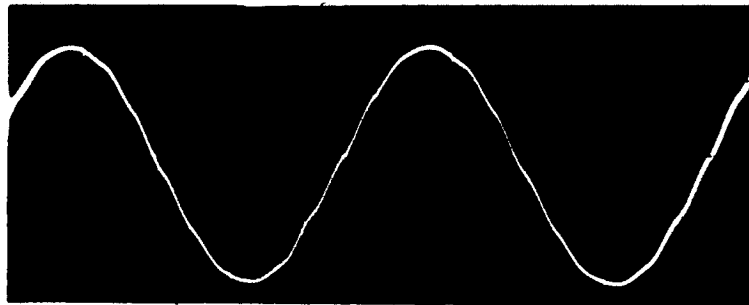
An analytical model for output distortion analysis is presented in Appendix D which relates output distortion to characteristics of the output filter (element 58) and the six power converter circuits (elements 52 - 57). This model is illustrated by the flow diagram in Figure D-1.

Distortion arises from the method of generating the waveform. This was described in detail in Reference 1. In brief, rectangular waves are summed to synthesize stepped waveforms which approximate sinusoids and the harmonics of the 400 cps fundamental component are attenuated by the output filter. The synthesis process is illustrated in Figure D-2 for one of the three phases. Oscillograms of the actual stepped waveform and the output waveform taken with the inverter breadboard circuit are shown in Figure 5. The stepped waveform represents the voltage across one leg of the delta connection of the secondary windings of the power transformers and with the output filter disconnected. The output waveform represents the same stepped waveform after filtering.

The ideal stepped waveform is defined as the waveform having step levels which minimize the harmonic distortion. These ideal step levels were derived in the appendix of Reference 1 for a twelve-step waveform as



Stepped Waveform (Output Filter Disconnected)



Output Waveform (Measured Distortion = 1.6%)

Vertical Scales: 100 V per div.

Horizontal Scales: 0.5 msec per div.

Figure 5 . Inverter Output Waveforms Before and After Filtering (Full-Load Conditions)

shown in Figure 5. With two steps within a period at zero, the other steps occur at relative levels of 1.0, 1.732, and 2.0. A closed form solution for distortion in Reference 1 for the ideal waveform resulted in 15.25% as the minimum possible distortion.

For considering the effects of filtering, a finite Fourier series representation is required. The model in Appendix D is limited to the fundamental frequency component and the first 39 harmonics. Distortion of the ideal stepped waveform computed in this manner is 13.86%. To obtain a reference value for distortion of the filtered waveform, nominal characteristics of the output filter parameters and full resistive load conditions of the inverter are assumed. Including the first 39 harmonics, the 13.86% distortion is reduced by the filter to 1.53%. In comparison, measured distortion of the output waveform in Figure 5 is 1.60%.

Except for special failure modes of certain circuits the sources of distortion contributing to the reference value are

- (i) switching transients in the power converter stages,
- (ii) ripple on the controlled dc bus from the primary voltage regulator,
- (iii) deviation of the step levels from the nominal values specified by the ideal stepped waveform, and
- (iv) variations in the characteristics of the output filter.

In the oscillogram of the actual stepped waveform in Figure 5, the voltage spikes on the leading edges of the steps when viewed on an expanded horizontal scale are identified as switching transients with the major frequencies at 100 kc or greater. Filter transfer function characteristic are introduced later and from these it is obvious that attenuation at these frequencies (-36 db or greater) renders these transients negligible as contributions to output distortion.

The smoothness of the oscillogram trace of the stepped waveform also makes it obvious that ripple on the controlled dc is a negligible source of distortion. 9.6 kc ripple is introduced by input current switching in the primary voltage regulator; however, this is adequately attenuated by the LC filter following the switching transistors. In an experimental determination of failure mode effects, capacitors C6 and C7 were disconnected (simulating open modes) and inductor L4 shunted out (simulating a short). The measured output distortion was less than 4% which is still within the 5% requirement.

Deviation of step levels as described under (iii) above are assumed to result from variation in part characteristics of the power converter circuits. A schematic diagram of the power converter No. 1 is presented in Figure 45. The analytical model in Appendix D relates the step levels to parameters of all six converter circuits to include the effect of variations both within each circuit and among the circuits. The assessment of contributions to distortion from these circuits was a calculation for worst-case conditions. Parameter values and variations are listed in Table VIII. R_{iU} and R_{iL} represent resistances of the two primary windings (upper and lower as in Figure 45) for the i -th circuit. The nominal value of 0.4Ω represents the average of measurements for the six transformers in the breadboard. The $\pm 0.12 \Omega$ variation is a pessimistic worst-case assumption. V_{siU} and V_{siL} similarly represent collector-to-emitter saturation voltages with the nominal value and assumed worst-case variations selected as typical from manufacturer's data. As described in Appendix D, worst-case conditions occur when there are no reactive currents; therefore, voltage drops of the diodes (see Figure 45) are not necessary. 2.50 amp for exciting current I represents typical full load (and worst-case) conditions and 20.75 v is a typical measured value of V_C which varies only slightly with load. The six power transformers are considered adequately matched so that variations among transformers are negligible. Furthermore, the core losses are considered sufficiently small so that the three voltage transformers adequately represented by the turn ratios a_1 , a_2 , and a_3 .

Using the relationships in Appendix D, it was determined by manual calculations that the worst-case variations listed in Table VIII contribute at most, an added 1.5% to the 15.26% total distortion as computed for the ideal stepped waveform. Filtering renders this additional distortion negligible.

The latter possible source of contribution to distortion stated in (iv) above is the variation in the output filter characteristics. Voltage gain vs. frequency characteristics computed with the output circuit modeling equations in Appendix A are shown in Figure 6. As described in Reference 1, two transfer functions are involved, one for values of $n = 3k - 2$, $3k - 1$ and another for $n = 3k$ ($k = 1, 2, \dots$), because of the inherent phase relationships of the harmonics in the three phases. It was also shown in Reference 1 that harmonics of the ideal stepped waveform having twelve steps occur only at $n = 12 \ell + 1$ ($\ell = 1, 2, \dots$) which does

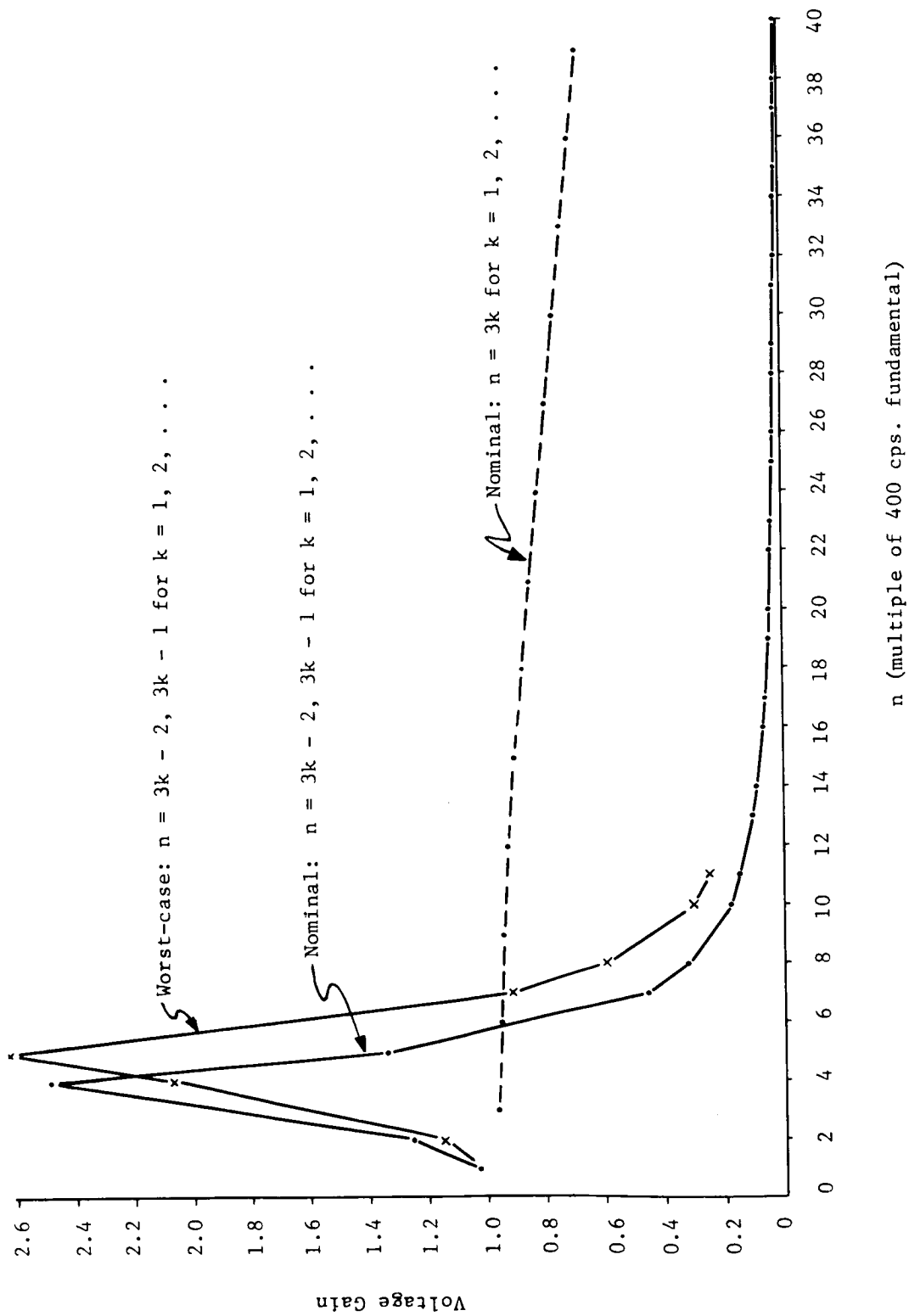


Figure 6. Output Filter Voltage Gain vs. Frequency

TABLE VIII

Circuit Parameter Variations for Distortion Analysis

<u>Parameter</u>	<u>Nominal Value</u>	<u>Variation</u>
R_{iU}, R_{iL}	0.4 Ω	$\pm 0.12\Omega$
V_{siU}, V_{siL}	0.6v	$\pm 0.1v$
V_C	20.75v	--
I	2.50 amp.	--
a_1	$\frac{370}{180}$	--
a_2	$\frac{276}{180}$	--
a_3	$\frac{94}{180}$	--

not include any of the $n = 3k$ values. Application of the other portion, i.e., for $n = 3k - 2$, $3k - 1$, of the nominal characteristic to the components of the ideal stepped waveform results, as reported above, in 1.53% output distortion.

To assess the effects of output circuit parameter variation or distortion, a worst-case condition is sought which is the characteristic that yields the least attenuation of harmonics. The voltage gain plot labelled as worst-case in Figure 6 is assumed to represent this condition and was obtained as follows:

In earlier discussions on output voltage and phase imbalances, a statistical design was described for computing worst-case imbalances due to variations in output circuit parameters, and this involved calculations for the fundamental frequency ($n = 1$) only. Calculations with this design were extended through frequencies of $n = 11$ to obtain an indication of possible worst-case filter characteristics, and the result is the characteristic plotted in Figure 6 for values of $n = 3k - 2$, $3k - 1$. For values of $n = 3k$, changes from the nominal voltage gains were insignificant. The

worst-case characteristic resulted from the conditions when the inverter load was resistive and all circuit parameter values were decreased by the assumed maximum variation.

The basic form of the transfer function (a quadratic filter) thus remains unchanged and the variation is essentially a translation to higher gains. The increase in gain is, at most, a factor of two (+ 6db) near the resonant peak and decreasing to 1.6 (+ 4db) at $n = 11$, the first harmonic in the ideal stepped waveform. At higher frequencies the increase settles to a constant factor of about 1.2 (+ 2db) due to the increase in resonant frequency from 1600 cps to 2000 cps. Assuming for worst-case calculations a constant increase of +4 db for all $n \geq 11$, the output distortion from filtering the ideal stepped waveform with the worst-case filter is computed to be 2.5% which is still well within requirements.

From the investigations described above, none of the sources of contribution to output distortion individually cause failure to meet the requirements of 5%. The greatest contribution results from parameter variations in the output circuit and the other three were adjusted negligible.

Failure modes of certain circuits and their effect on output distortion are of special interest. First, as described earlier, it was determined experimentally that removal of the filter in the primary voltage regulator to simulate failures of filter components does not result in failure to meet requirements. The existence of many undesirable transients in the power converter without this filter precludes its complete removal from the circuit.

It is also of interest to consider the effect on output distortion of disabled timing channel circuits such that drive to the primary windings of the power transformers T1 - T6 is lost. With reference to Figure D-2 and the equations in Appendix D, the effect can be assessed in a gross manner by setting individual voltages V_1 through V_6 at zero one at a time and computing the distortion of the resulting waveform with the missing steps. Considering consecutively V_1 , V_2 , and V_3 , i.e., the large, intermediate, and small steps, as zero results in 20.0%, 12.2%, and 3.9% respectively for output distortion using the nominal filter characteristics. The same calculation for V_4 , V_5 , and V_6 results in the same three values for the loss of the respective large, intermediate, and small steps.

In the failure modes and effects analysis, it is shown that some component failures in the timing channel can cause complete failure of the

inverter if the component failure causes the controlled dc bus to be shorted to ground. Simple disabling of the circuit is also possible for certain component failures, as for example, the output lead of the flip-flops in the pulse sequence generator becoming disconnected so that drive is lost. Setting the steps to zero in the manner described above requires the assumption that no voltage is induced in the appropriate transformer secondary winding by currents through the other two windings. If the transformer cores become saturated, the assumption is valid; however, experimental results indicate this is not the case.

To more realistically assess the effects, individual timing pulse amplifiers were disabled in the inverter breadboard to cause loss of drive to a power converter and output distortion observed for the three channels. The results are presented in Table IX. These are not consistent with the analytical results in terms of actual values, however, the relative values are in the anticipated order. This order is designated by the appropriate values in parentheses beside each experimental value. The greatest source of deviation from the analytical results is probably the induced voltages in the secondary windings as described above. The deviation among values for equivalent high, intermediate and low levels, is probably due to the same effect coupled with the created voltage imbalance among the three phases. The effect of disabled timing channel circuits on voltage imbalance was not investigated in detail, however, it can be shown analytically that a disabled timing channel leads to either condition of one phase voltage lower than nominal with the other two higher than nominal and approximately equal in value or two phase voltages lower than nominal and approximately equal in value with the other higher than nominal. To illustrate the effect, the results of breadboard measurements with disabled timing channels are presented in Table X. The average of the three values for each condition is also listed and the deviation from the 115 vac nominal indicates there is some effect on voltage regulation. Actual values of phase voltages are thus affected by the voltage regulation loop operation; however, the order of the relative values predicted by analytical treatment is correct.

The greatest distortion in Table IX for this failure mode is 32%, more than six times the rated 5% requirement and only one, the 3.3%, is within requirement. For some inverter applications these distortions may be acceptable; however, the decision for acceptability of the inverter

TABLE IX

Measured Output Distortions With Disabled Timing Channels

Disabled Timing Channel	Per Cent Distortion		
	<u>Phase AB</u> (%)	<u>Phase BC</u> (%)	<u>Phase CA</u> (%)
1	16.6(20.0)	5.3(3.9)	14.4(12.2)
2	10.0(12.2)	9.0(3.9)	24.7(20.0)
3	5.2(3.9)	9.2(12.2)	16.3(20.0)
4	3.3(3.9)	25.0(20.0)	9.2(12.2)
5	10.3(12.2)	17.2(20.0)	7.2(3.9)
6	32.0(20.0)	9.8(12.2)	8.4(3.9)

TABLE X

Measured Phase Voltages With Disabled Timing Channels

Disabled Timing Channel	Phase Voltages			Three Phase Average
	<u>Phase AB</u> (volts)	<u>Phase BC</u> (volts)	<u>Phase CA</u> (volts)	
1	91	145	93	109.7
2	140	136	64	113.3
3	154	94	97	115.0
4	145	69	145	119.7
5	98	92	155	115.0
6	66	134	140	103.3

performance during this failure mode should also include the voltage imbalance and average three-phase voltage.

(f) Input Current Modulation

Since requirements on input current modulation are undefined, treatment of this attribute was limited to elementary analytical investigations and several observations with the breadboard circuit. The factors of primary interest are the input voltage source characteristics, the inverter load, and the inverter input filter contained in the primary voltage regulator circuit (see Section 3.3.4.16). For the analytical investigations, a Thevenin's equivalent circuit was assumed for the source with source impedance ranging from 1 to 3 ohms, perfect switching in the inverter was assumed, and the effect of the output filter of the primary voltage regulator was neglected. Computed input current modulation (peak-to-peak) using nominal input filter characteristics was found to be less than 1% for the full range of load conditions. In comparison, the maximum peak-to-peak modulation observed experimentally was less than 2%.

Further investigation could be extended to considering the effects of circuit parameter investigation, but in view of the small magnitude of modulation and the undefined requirements, additional efforts was not considered justified. If it could be confirmed that increased modulation will not cause detrimental effects on the sources or other circuits connected to it, then the amount of input filtering could be decreased.

(g) Power Dissipation

Attention to power dissipation of individual components to assure capabilities are not exceeded is given in the components stress analysis of Section 3.3.1.1 with further considerations in the individual Sections 3.3.4.1 through 3.3.4.16.

Estimates for the total power dissipation of the circuit can be obtained by summing estimates for individual components; however, a more realistic method is to rely on measurements of input and output voltages and currents using the breadboard circuit.

Results of breadboard measurements for both resistive and reactive loads are summarized in Figures 7 and 8 for the full range of normal load conditions. As described in Section 3.3.4.10, the reactive load of 160Ω with a reactive angle of +45 deg. represents the load conditions for maximum efficiency of operation. In the upper graphs input currents are plotted for extremes of input voltage of 25 vdc and 30 vdc and ambient temperature of 0°C and 100°C. These currents were used to compute input powers ($V_{in} \times I_{in}$) plotted in the

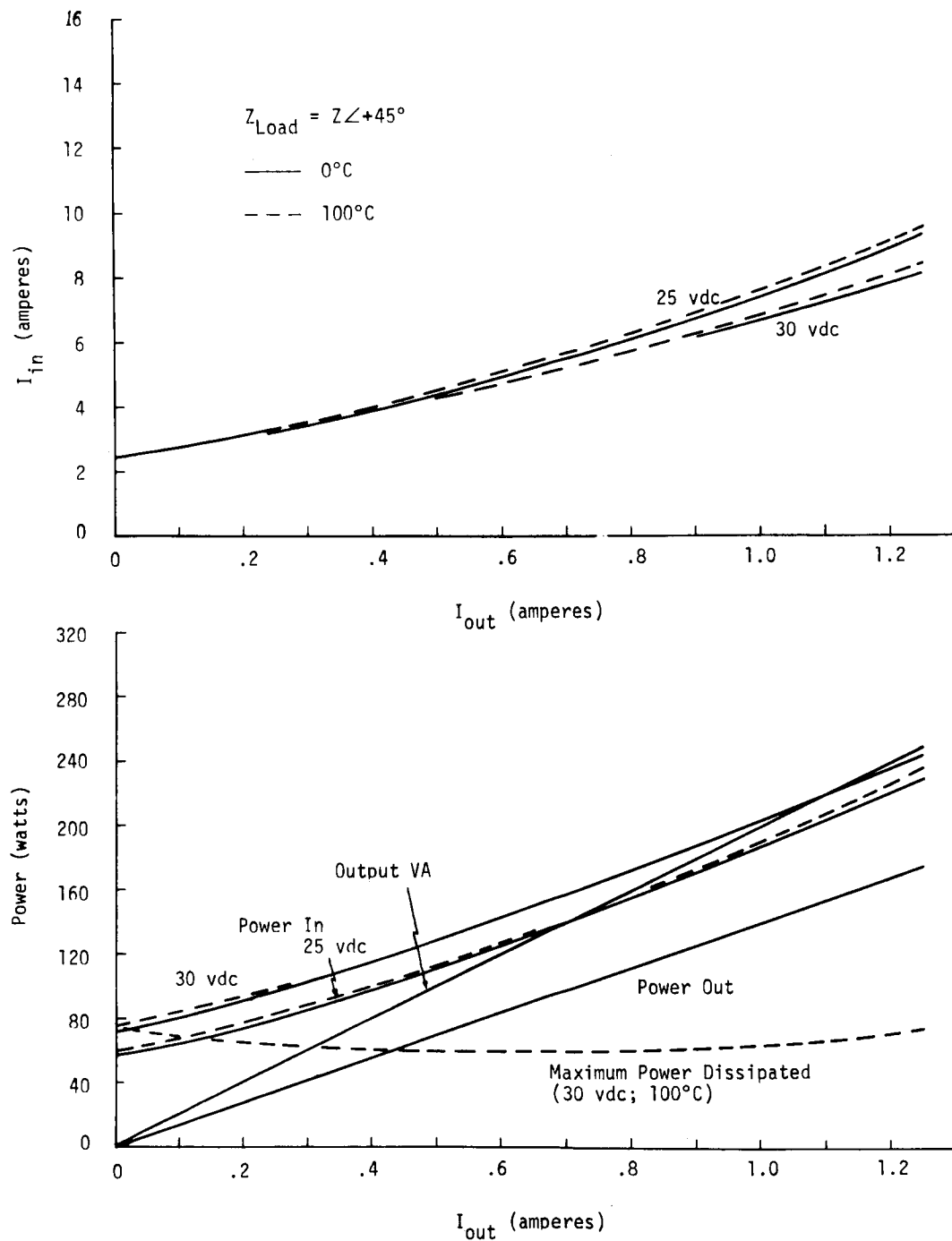


Figure 7. Power Curves for Balanced Resistive Load

lower graphs. Output power values plotted in the lower graphs were computed by $3 \times 115 \text{ vac} \times I_{\text{Load}} \times \cos 45^\circ$ where I_{Load} represents the current per phase and $I_{\text{Load}} = I_{\text{out}} \sqrt{3}$.

Maximum power dissipation as plotted in the lower graphs are simply the differences of maximum input power (30 vdc input at 100°C) and output power. Dissipation is greater for resistive loads with a maximum of 140 watts at full load. Minimum efficiencies for resistive load range from 0 at no load to 64% at full load. Maximum power dissipation for the reactive load is 75 watts at full load with minimum efficiencies ranging from 0 at no load to 59.5% at half load to 71% at full load. The 71% meets the design goal of 70% stated in Section 3.2.2.4 for full load operation.

From the upper graphs in Figures 7 and 8, the maximum input currents for normal operation are 15 amp. for resistive loads and 9.5 amp. for the reactive loads. Both are well within the 20 amp. requirement stated in Section 3.2.2.2.

(h) RF Interference

Since assessment of RF interference is more easily performed experimentally with packaged models of the circuit, extensive analysis were not performed in this effort. Limited consideration of the effects of RF interference on operation of integrated circuits is described in Section 3.3.4.4.

(2) Turn-On, Turn-off, Transient Response, Overload, and Load Start Modes Presented in Section 3.3.3.2 and 3.3.3.3.

3.3.2 Analyses for Circuit Sections

The first level of breakdown of the complete inverter circuit into the timing section and the control and conversion section recognizes two distinct circuit operations. A functional diagram illustrating their relationship is presented in Figure 9. The major power conversion of the unregulated dc is performed in the control and conversion section which also provides regulation of the output voltage. The 400 cps timing signals from the timing section govern the switching sequence of the power converter stages and 4.8 kc excitation is also supplied by the timing section to the magnetic amplifier.

Detailed analyses of these sections are more efficiently performed at still lower levels of breakdown; however, the implications of the functional operation of these sections on the analyses are described below.

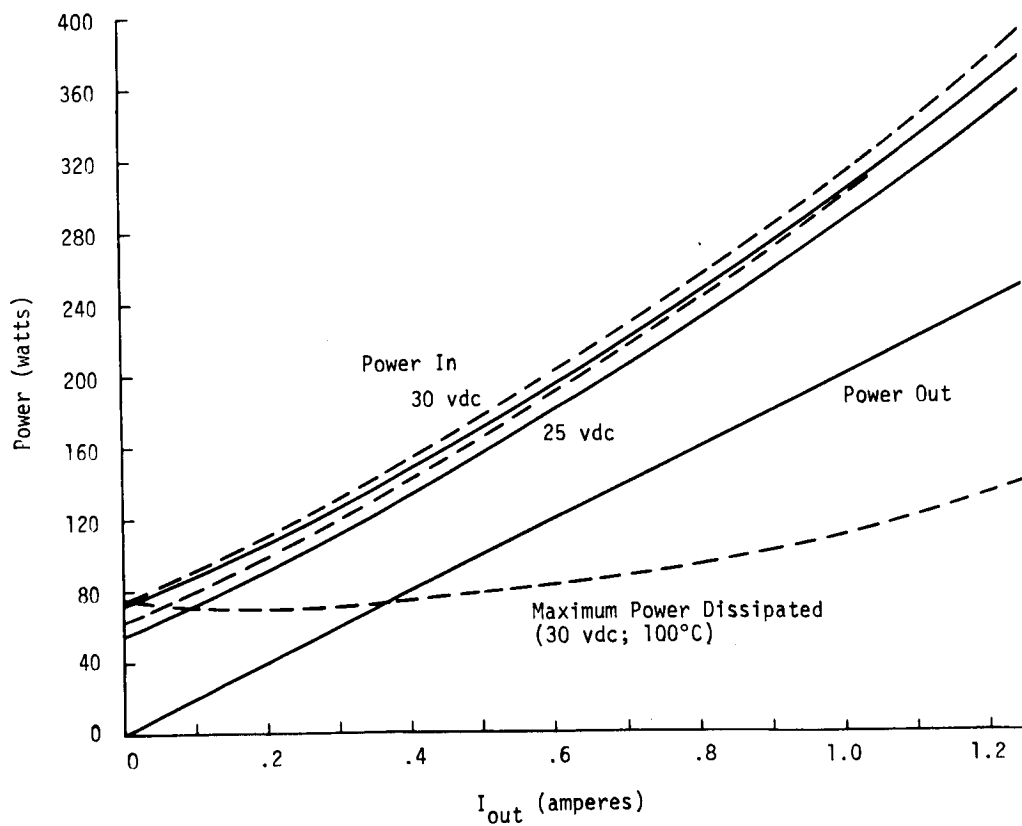
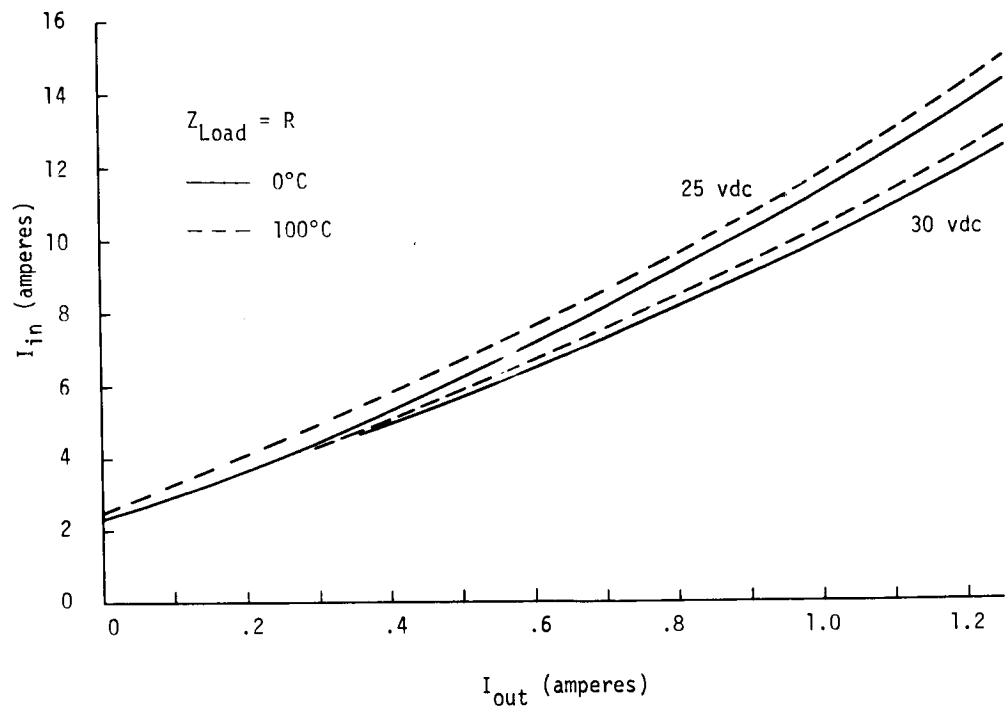


Figure 8. Power Curves for Balanced Reactive Load

3.3.2.1 Timing Section (Element 11)

The function of this element during all operating modes is to supply the timing signals and magnetic amplifier ac excitation as illustrated in Figure 9. The characteristics of major interest for these signals is frequency, ON and OFF current levels, and switching transients. Along with power dissipation and RF interference, these characteristics are designated as performance attributes of the timing section and all are discussed separately below.

(1) Frequency

Due to the manner of generating the output waveform, the timing signal frequency uniquely determines the inverter output frequency and thus the same requirements on stability apply. As described in Section 3.3.1.4, this frequency is directly related to operation of the primary oscillator circuits which are discussed in Section 3.3.4.3. The magnetic amplifier ac excitation frequency is also directly related to the operation of these circuits, the frequency stability requirements of which are more than adequate for the magnetic amplifier ac excitation.

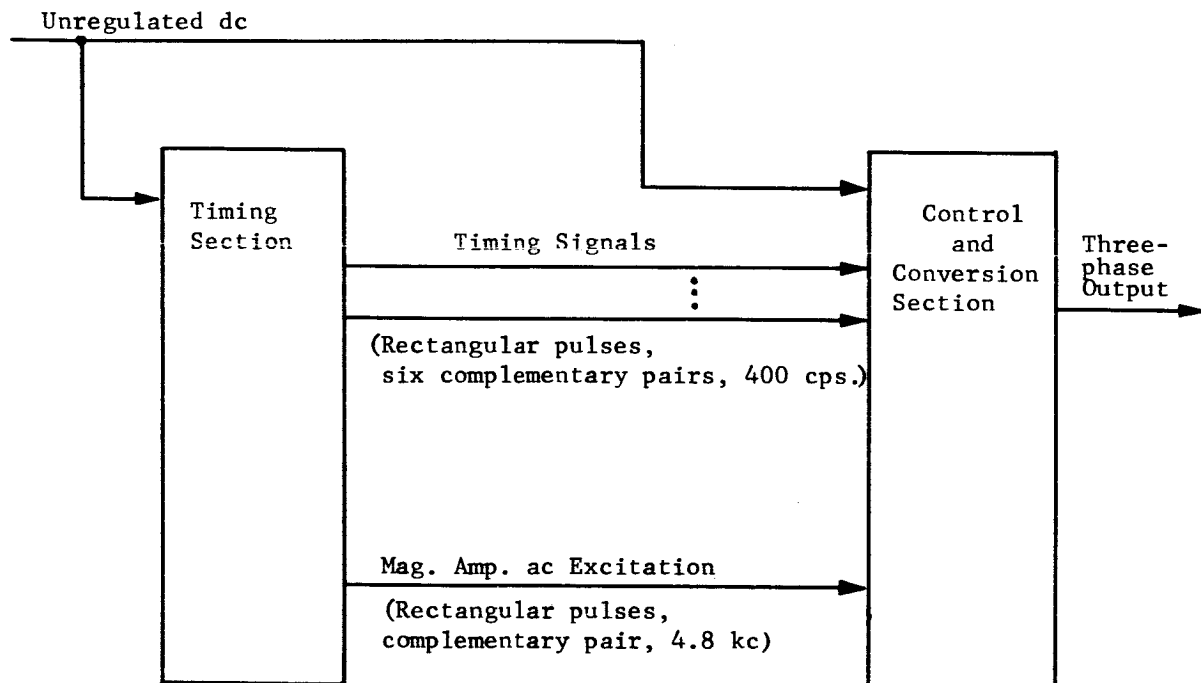


Figure 9. Functional Diagram for Circuit Sections of the Inverter

(2) ON and OFF Current Levels

The timing signals provide base drive to power switching transistors in the power converter circuits in the control and conversion section. For nominal operation it is required that the transistors be driven well into saturation during the required ON period and non-conducting during the required OFF period.

The output circuits in the timing section supplying these signals are the timing pulse amplifiers. Worst-case analyses in Section 3.3.4.9 show that ON level currents are adequate within the probable range of variation. Also, the base-emitter junction of the switching transistors are reverse biased so that OFF level currents are adequate.

The magnetic amplifier ac excitation is similarly employed as base drive to switching transistors in the magnetic amplifier driver circuit and is supplied by integrated circuit flip-flop units as shown in Figure 54. Performance variation studies in Reference 3 suggest a modification of the magnetic amplifier driver circuit. The original and modified circuit provide adequate current levels. It is possible that the magnetic amplifier ac excitation can be absent due to failure of the driving flip-flop shown in Figure 54 while the timing section is still supplying timing signals. However, complete failure of the inverter would result from this event and was included in the logic model for reliability prediction in Section 3.3.1.1.

(3) Pulse Transients

As described in Section 3.3.4, effects of transients on performance for all switching applications in the inverter circuit are considered insignificant due to the relatively low switching frequencies involved.

(4) Power Dissipation

Power dissipation for the timing section was treated collectively with that for the control and conversion section in Section 3.3.1.4 and is considered adequate for this stage of design.

3.3.2.2 Control and Conversion Section (Element 12)

The function of this element is to provide the major power conversion from dc to ac as governed by the timing signals and voltage regulation loop. With the exception of power dissipation and RF interference, the attributes and requirements are the same as those defined and discussed for the complete inverter circuit in Section 3.3.1.4. Power dissipation and RF interference are treated collectively in Section 3.3.1.4 with like characteristics of the timing section.

3.3.3 Analyses for Major Circuits

The major circuits are the timing generators and the voltage regulation and overcurrent protection loops in the control and conversion section. Analyses of these are described below.

3.3.3.1 Timing Generators A and B (Elements 16 and 17)

These operate in standby redundancy [Ref. 1]. Their functional relationship to other elements of the timing section is illustrated in Figure 3. In brief, the output of the active generator is used to excite an electronic switch which blocks the application of power to the other generator leaving it inactive. In the event of failure of the active generator the loss of excitation to the electronic switch permits power to be applied to the previous inactive channel.

The function of these elements is to generate the six complementary pairs of rectangular 400 cps. pulses as timing signals and a complementary pair of rectangular 4.8 kc pulses as excitation for the magnetic amplifier. The output portion of the timing generators consist of integrated circuit flip-flops which do not have adequate power capability to drive the power converter stages. The timing pulse amplifiers are employed to provide the necessary amplification for the timing signals and the magnetic amplifier driver circuit for the magnetic amplifier ac excitation. Output pulse frequency, ON and OFF current levels of the output pulses, pulse transients, power dissipation and RF interference are attributes of major concern. For performance consideration these are all treated with other elements. Designation of these elements had greatest utility in logic models for reliability prediction.

3.3.3.2 Voltage Regulation Loop (Element 18)

This analysis illustrates performance variation studies for the portion of the inverter circuit which determines the behavior of the following attributes:

Normal Operation Mode

Average three-phase output voltage

Transient Response Mode

Maximum voltage deviation during a transient

Transient time

Turn-on Mode

Output voltage overshoot

Turn-on time

Turn-off Mode

Turn-off time

The function of the voltage regulation loop is to provide regulation of the output voltage over the full operating range of load and input voltage. The transient response of the loop is also of interest.

The voltage regulation loop is defined by the major loop in the functional diagram of Figure 10. Even though some of the circuits are digital, the over-all operation is analog. The basic approach to analysis was to first model the attributes as functions of characteristics of circuit parts, input voltage and load. Both analytical and empirical techniques have been employed in the modeling effort.

Circuit analyses provided the following differential equations for describing the transient response of the loop.

Forward Loop (Involving elements 52 - 58 and 64):

$$\frac{d^2V}{dt^2} + A_1 \frac{dV}{dt} + A_0 V = B_0 + B_1 V_{in} \tau \quad (12)$$

Feedback Loop (Involving elements 59 and 63):

$$\frac{d\tau}{dt} + k\tau = C_1 + C_2 V \quad (13)$$

In the above equations, V is the average three-phase output voltage (see Section 3.1.2); τ , pulse width of the magnetic amplifier output pulses; t , time; V_{in} , input voltage; and the coefficients A_0 , A_1 , B_0 , B_1 , C_1 , C_2 , and k are complicated functions of the circuit part characteristics and are defined explicitly in Appendix B. The characteristics of the inverter load are included in the coefficients A_1 , B_0 , and B_1 .

With $V_{in} \tau$ in Equation (12) treated as a single variable, each of the above equations is linear; however, because of the product term, the system described by both equations is non-linear. These equations were derived and their assumptions given previously [Ref. 8 and 9]. In general, the assumptions linearized the transfer characteristics of individual circuits to allow analysis. For certain cases, the simplifications led to results not descriptive of the actual circuit operation; however, the derivation is justified by the depth of familiarity it provided for actual circuit operation, contributing greatly to the assurance for reliable design.

Use of equations (12) and (13) in analyzing for the behavior of specific inverter attributes is described below.

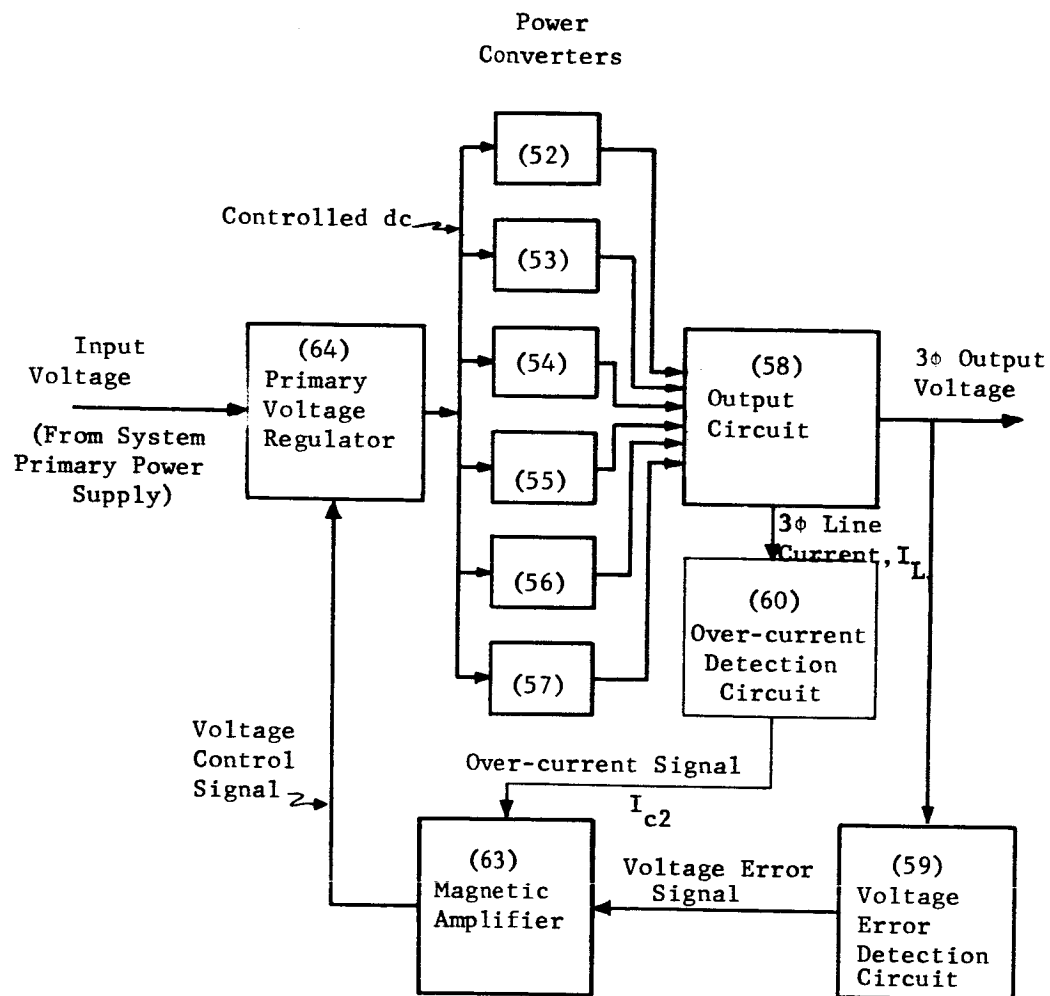


Figure 10. Functional Diagram for the Voltage Regulation and Over-current Protection Loops (Elements 18 and 19)

(1) Normal Operation Mode--Average Three-phase Voltage

The simultaneous solution of (12) and (13) for steady-state conditions is

$$V_{ss} = \frac{kB_o + B_1 C_1 V_{in}}{kA_o - B_1 C_2 V_{in}}. \quad (14)$$

With the coefficients expressed as functions of the load and circuit part characteristics, (14) provides a model of the general form,

$$V_{ss} = g(R_{73}, R_{74}, V_z, \dots, V_{in}), \quad (15)$$

for investigating the output voltage regulation. The model is used to perform end-limit studies to investigate for sensitivity, non-linear and interaction effects, and worst-case performance values; and statistical distribution studies to investigate correlation effects and performance distribution characteristics. In addition, tests with the breadboard circuit were conducted to supplement the analytical studies. All studies and results are described in more detail below.

(a) End-limit Studies

The use of end-limit techniques are described in detail in Vol. I, and the model expressed by Equation (14) was used in that description in a sample application. The computations required for obtaining the results discussed below were presented in Vol. I and will be referred to as appropriate.

The nominal values and the variations of circuit parameters used in the computations are tabulated in Table XI. In general, the part variations presented were selected to represent absolute maximums. The parameter α , representing the relative position of the potentiometer arm of R_{74} , was set at the value which provided 115 v for V_{ss} with all independent variables at nominal and half-load inverter conditions. The input voltage variation of $\pm 16\%$ allows a 23.5 to 32.5 v range of variation. Load impedance z_L and the number of turns in the magnetic amplifier windings N_f were treated parametrically as indicated. The listed values of load impedance included the range from no load ($z_L = \infty$) to full load ($z_L = 160\Omega$). N_f was varied to investigate for optimum loop gain. The feedback windings, through positive feedback action, directly affect the gain of the magnetic amplifier circuit which, in turn, contributes to overall loop gain. For $N_f = 0$ the magnetic amplifier gain is high with it increasing to still larger values with increasing N_f .

It is shown in Vol. I how the expansion of a function such as (15) into the initial terms of a Taylor series expansion assists in defining and interpreting re-

TABLE XI

List of Independent Factors for the Average
Three-phase Steady-state Output Voltage Model

<u>Factor</u>	<u>Nominal</u>	<u>Deviation (Δx_i)</u>
C	2 μ f	$\pm 15\%$
C _R	2000 μ f	$\pm 15\%$
K _{ϕ}	2.18×10^{-3}	$\pm 10\%$
L	1.65 mh	$\pm 6\%$
L _R	0.23 mh	$\pm 6\%$
N _{cl}	1000 turns	fixed
N _f	--	0, 1, 2, 3, 4 turns
N _g	250 turns	fixed
N _{sh}	10 turns	fixed
R' _g	104 Ω	$\pm 5\%$
R ₆₇	150 Ω	$\pm 5\%$
R ₆₉	145.7 Ω	$\pm 5\%$
R ₇₃	1.1 k Ω	$\pm 5\%$
R ₇₄	200 Ω	$\pm 5\%$
R ₇₅	20 k Ω	$\pm 5\%$
R _p	0.40 Ω	$\pm 3\%$
R _s	4.8 Ω	$\pm 3\%$
R _{sh}	0.15 Ω	$\pm 2\%$
R _w	100 Ω	$\pm 4\%$
T	104.27 μ sec	fixed
V _{ces}	1.0 v	$\pm 5\%$
V _g	12.0 v	$\pm 7\%$
V _{in}	28 v	$\pm 16\%$

TABLE XI (continued)

List of Independent Factors for the Average
Three-phase Steady-state Output Voltage Model

<u>Factor</u>	<u>Nominal</u>	<u>Deviation</u> (Δx_i)
V_z	8.4 v	$\pm 5\%$
z_L	--	160, 320, 1600, 16000, $\infty \Omega$
α	--	$0 < \alpha < 1$ (adjustable)
ϕ_K	-3.23×10^{-6}	$\pm 5\%$
ϕ_S	3.0×10^{-6}	$\pm 5\%$
ω	$2\pi \times 400$ rad./sec.	fixed

sults of computations with the model. Expanding (15) about the nominal output voltage V_N to include second-degree terms,

$$\begin{aligned}
 V_{ss} = V_N + \sum_{i=1}^n \left(\frac{\partial V_{ss}}{\partial x_i} \right) \Delta x_i + \sum_{i=1}^n \left(\frac{\partial^2 V_{ss}}{\partial x_i^2} \right) (\Delta x_i)^2 \\
 + \sum_{i=1}^{n-1} \sum_{j=i+1}^n \left(\frac{\partial^2 V_{ss}}{\partial x_i \partial x_j} \right) \Delta x_i \Delta x_j
 \end{aligned} \quad (16)$$

where x_i denotes the i -th of the n independent variables in the model with the deviation Δx_i representing the variation from the nominal value. Dividing (16) by V_N ,

$$\begin{aligned}
 \frac{V_{ss}}{V_N} = 1 + \sum_{i=1}^n \left(\frac{\partial V_{ss}}{\partial x_i} \right) \frac{\Delta x_i}{V_N} + \sum_{i=1}^n \left(\frac{\partial^2 V_{ss}}{\partial x_i^2} \right) \frac{(\Delta x_i)^2}{V_N} \\
 + \sum_{i=1}^{n-1} \sum_{j=i+1}^n \left(\frac{\partial^2 V_{ss}}{\partial x_i \partial x_j} \right) \frac{\Delta x_i \Delta x_j}{V_N}
 \end{aligned} \quad (17)$$

This normalized form reveals the relative contribution of each term to the deviation from the nominal value.

Using the variations presented in Table XI for the Δx_i 's, Equation (14) was employed directly to evaluate the individual terms in Equation (17). This computation was performed for all values of z_L and N_f listed in Table XI with α readjusted as described above for each value of N_f .

The contributions of the linear terms to output voltage variation is summarized in Figure 11. The log plot contains three orders of magnitude for the relative contributions. The variables listed in Table XI, but which are not represented in Figure 11, all had relative contributions less than those shown and were thus considered insignificant. The three most significant contributions of the quadratic term are shown similarly plotted in Figure 12 for the four values of N_f . Comparison of each with the corresponding linear term value in Figure 11 shows that each differs from the linear term values by an order of magnitude. The linear term values in Figure 11 are thus considered adequate to represent one-at-a-time variations or sensitivities of output voltage to variations in individual circuit parameters. Experimental check of the sensitivities was performed with breadboard circuitry, and, in general, good agreement was obtained. This is discussed further and comparisons made later in this section.

By definition, sensitivity values plotted in Figure 11 are directly dependent upon the part variations listed in Table XI. As previously mentioned, the variations were selected to represent absolute maximum variations. The variations were not related to all possible sources and conservative values were selected to collectively include all effects. With more realistic values, the results can be readily updated by adjusting the values in direct proportion to the new variations selected.

With reference to Figure 11, the variables V_z , R_{73} , and R_{75} are, by far, the most sensitive, individually causing output voltage variations in excess of 4%, but these do not change with N_f . The corresponding components are located in the voltage reference section of the voltage error detection circuit. The difference in sign between R_{73} and R_{75} tends to cancel the effect of their variation if there is high correlation between them. The significance of these results on component selection is discussed in Section 3.3.4.11.

The sensitivity of the output voltage to changes in V_{in} , the input voltage, is considerably less than that for V_z , R_{73} , and R_{75} but is highly dependent on N_f . An increase in N_f results in an increase in loop gain, and the dependence of V_{in} on sensitivity to N_f is shown in Figure 11. This illustrates the desirability of providing a loop gain as high as possible so long as other factors such as loop stability and damping characteristics are satisfactory. The resulting output voltage variations

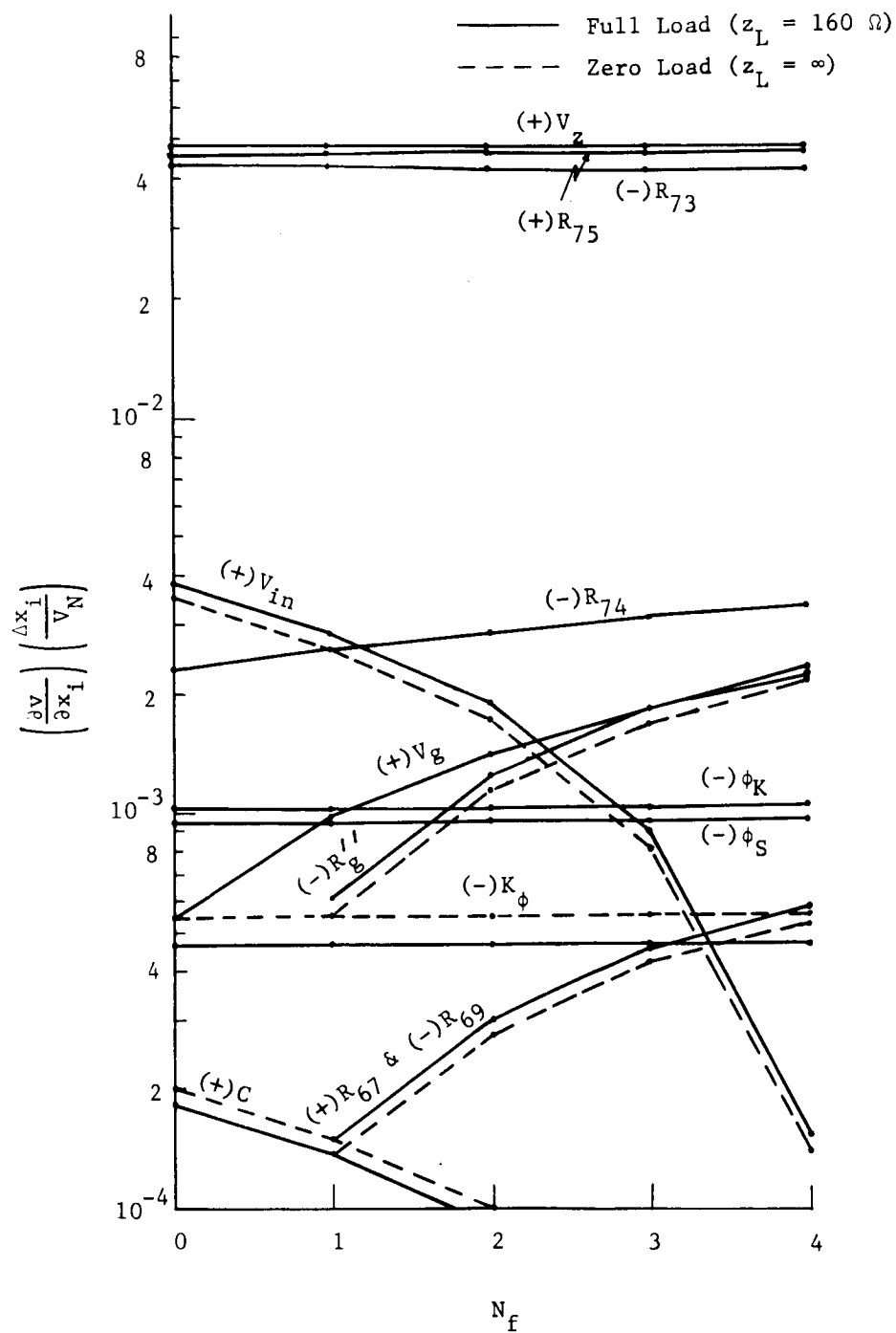


Figure 11. Plot of First-order Variations of Output Voltage vs. Loop Gain Parameter, N_f .

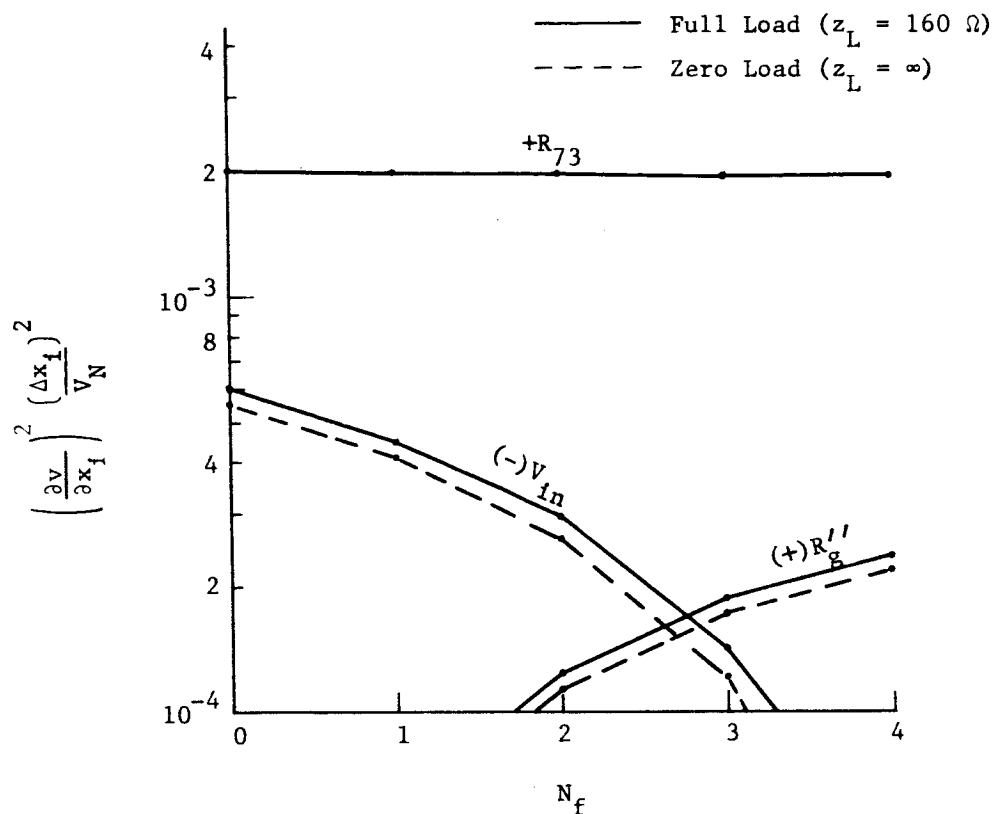


Figure 12. Plot of Second-order Variations of Output Voltage vs. Loop Gain Parameter, N_f .

are less than 0.4% for $N_f = 0$ and decrease to less than 0.02% for $N_f = 0$ over the full range of load conditions from $z_L = \infty$ to $z_L = 160\Omega$. This indicates more than adequate regulation capability of the voltage regulation loop. These results are later compared to similar experimental results.

In the inverter design, a goal has been to provide the highest regulation loop gain possible by increasing the positive feedback in the magnetic amplifier circuit. As illustrated in Figure 11, the sensitivity of some variables increases with increased gain, for example, C . Others, such as the K_ϕ sensitivity are not affected, and some sensitivities increase with increasing N_f . If these variations are as equally

likely as variations in V_{in} then their combined effect offsets the advantage stated for high gain. This may allow definition of an optimum gain which minimizes the combined effect of all variations.

An optimization criterion used in communication theory selects the gain which minimizes the mean square error (or variation from nominal) in the output voltage. This computation is that performed with the moments method for distribution studies and is described later.

Interaction effects are represented by the cross-product terms in Equation (17). These were computed for $N_f = 3$ only and the most significant contributions for this case are listed in Table XII. The values listed are an order of magnitude less than the corresponding linear terms indicated for either variable in Figure 11. A further check on the contribution of interaction effects is performed by absolute worst-case calculations as described below.

Absolute worst-case values of output voltage were computed with both the original form of the model expressed by Equation (14) and with a Taylor series approximation containing linear and quadratic terms (and not cross-product terms). Comparison of results from the two computations provides a check on the collective contribution of all interaction terms (and also all terms of degree three and higher). Results are presented in Table XIII for extreme values of load and N_f values. The righthand columns labeled "interaction check" presents the values obtained with the series approximation, and comparison of these with the absolute worst-case limits shows only minor contribution of terms other than the linear and quadratic.

TABLE XII

Variable Interaction Contribution to
Output Voltage Variations ($N_f = 3$)

<u>Variable Combination</u>	<u>Relative Contribution</u>
$R_{73}R_{75}$	-0.210×10^{-2}
$V_z R_{73}$	-0.212×10^{-2}
$V_z R_{75}$	0.226×10^{-2}
R'_g/V_{in}	0.295×10^{-3}

TABLE XIII

Worst-case Output Voltages

N_f	Z_L (ohms)	Nominal Voltage (ohms)	Absolute Worst-case		Interaction Check	
			Maximum Voltage (volts)	Minimum Voltage (volts)	Maximum Voltage (volts)	Minimum Voltage (volts)
0	160	114.90	99.05	132.9	98.17	131.9
	320	115.00	99.14	133.1	98.26	132.1
	∞	115.10	99.22	133.2	98.35	132.2
4	160	115.01	98.96	133.4	98.10	132.4
	320	115.02	98.97	133.4	98.11	132.4
	∞	115.02	98.98	133.4	98.12	132.4

The resulting output voltage variations obtained with the worst-case computations are much greater than the allowable ± 1.0 vac requirements. Much of the variation, of course, results from overestimates in selecting the variations in circuit parameters. Worst-case analyses usually lead to pessimistic results and simultaneous occurrence of all variations at their worst-case values is very unlikely. Failure to conform to requirements by this analysis does not invalidate the design. In some applications, actual variations of the magnitude obtained can be tolerated. Due to the nature of these results, they are considered of limited utility.

(b) Distribution Studies

Two major techniques were employed for considering effects of statistical distributions of circuit parameters; these were the moments method and Monte Carlo simulations. Both are described in Vol. I.

In the moments method an approximate linear model, i.e., the linear terms of Equation (17), of the output voltage was employed. The assumption that the independent variables are normally distributed is inherent in the method so that the distributions are combined by

$$\sigma_{V_{ss}}^2 = \sum_i \left(\frac{\partial V_{ss}}{\partial x_i} \right)^2 \sigma_{x_i}^2 + 2 \sum_{i=1}^n \sum_{j=i+1}^n \rho_{ij} \left(\frac{\partial V_{ss}}{\partial x_i} \right) \left(\frac{\partial V_{ss}}{\partial x_j} \right) \sigma_{x_i} \sigma_{x_j} \quad (18)$$

where σ_y represents the standard deviation of variable y , ρ_{ij} represents correlation coefficient of variables x_i and x_j , and all other symbols are as previously defined. Particularly, the partial derivatives are those computed in the end-limit studies described above and, in general, differ for different conditions of load and N_f values.

Computations of the standard deviation of output voltage were performed both with assumed correlations of certain part variations and by assuming part variations were independent. Before presenting the results, comments on the experience in specifying correlations are in order.

Correlation between two variables implies there is some degree of functional dependence between them. For example, the resistances of two resistors having similar construction, i.e., both are carbon film, and in the same environment may be expected to vary in a similar (but not necessarily identical) manner with changes in temperature. Or, several characteristics of a device such as current gain, collector-to-emitter voltage drop, and base-emitter current of a transistor may all be strongly correlated for changes in temperature. Data which is helpful for specifying correlation of part characteristics are sparse and the choice of correlations is necessarily subjective.

For the model of steady-state output voltage, eighteen variables are involved and detailed consideration of all correlations is unfeasible. Major interest was to include some reasonable correlations to determine if they produced any significant effects on output voltage variation. For this purpose, four levels of correlation were selected for specifying correlation coefficients. These are:

No correlation (variables are independent), $\rho = 0$;

Weak (but not negligible) correlation, $\rho = 0.3$;

Strong (but not linearly dependent) correlation, $\rho = 0.7$; and

Complete correlation (linearly dependent), $\rho = 1.0$.

Using the above criteria, the correlation coefficients among the variables were specified and all values are presented in Table XIV. Each variable is, of course, completely correlated with itself along the diagonal of the array. Thermal environment served as the major basis for designating correlation among the variables. As a general rule, all resistances were assumed strongly correlated ($\rho = 0.7$). Since the source of V_{in} is external to the inverter, it was assumed independent ($\rho = 0$) of all other variables. Manufacturer's data of the magnetic amplifier core material indicated insignificant change of K_ϕ with temperature; thus, K_ϕ was also assumed not correlated with other variables. The negative correlation coefficients of V_z and V_g with other variables reflect the effect of their zener diode sources decreasing with increasing temperature. ϕ_s is similarly known from magnetic amplifier core manufacturer's data to decrease with increasing temperature thus giving negative correlation coefficients with other variables.

TABLE XIV

Variable Correlation Coefficients

	R_{75}	R_{74}	R_{73}	V_{ces}	V_z	ϕ_S	K_ϕ	R_P	L	R_S	C	V_g	V_{in}	R_w	R''_g	ϕ_K	R_{69}	R_{67}
R_{67}	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	0.7	0.0	0.7	0.3	-0.7	0.0	0.7	0.7	0.3	0.7	1.0
R_{69}	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	0.7	0.0	0.7	0.3	-0.7	0.0	0.7	0.7	0.3	1.0	
ϕ_K	0.3	0.3	0.3	0.3	-0.3	-0.3	0.0	0.3	0.0	0.3	0.3	-0.3	0.0	0.3	0.3	1.0		
R''_g	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	0.7	0.0	0.7	0.3	-0.7	0.0	0.7	1.0			
R_w	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	0.7	0.0	0.7	0.3	-0.7	0.0	1.0				
V_{in}	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.0					
V_g	-0.7	-0.7	-0.7	-0.3	0.3	0.3	0.0	-0.7	0.0	-0.7	-0.3	1.0						
C	0.9	0.3	0.3	0.3	-0.3	-0.3	0.0	0.3	0.0	0.3	1.0							
R_S	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	0.7	0.0	1.0								
L	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.0									
R_P	0.7	0.7	0.7	0.3	-0.3	-0.3	0.0	1.0										
K_ϕ	0.0	0.0	0.0	0.0	0.0	0.0	1.0											
ϕ_S	-0.3	-0.3	-0.3	0.3	0.3	1.0												
V_z	-0.3	-0.3	-0.3	-0.3	1.0													
V_{ces}	0.3	0.3	0.3	1.0														
R_{73}	0.7	0.7	1.0															
R_{74}	0.7	1.0																
R_{75}	1.0																	

With slight modifications the listed coefficients represent initial best engineering judgments within the allotted effort for specifying them. As described in Vol. I, a requirement of a correlation matrix is that it be positive definite or positive semidefinite (the characteristic roots must be non-negative). This criterion provides a check on the physical possibility of the designated correlations. With the original array of correlation coefficients selected by engineering judgment only five minor modifications of specified values were required to achieve the array shown in Table XIV which satisfied this criterion.

For computing output voltage standard deviations, the Δx_1 variation listed in Table XI were used as a basis for specifying standard deviations of circuit parameters. First, letting the Δx_1 's represent 4σ values for variables, output voltage standard deviations were computed for $N_f = 3$ and half-load ($z_L = 320 \Omega$) conditions to compare results obtained with and without correlation. These results are:

(i) With variables correlated, $\sigma_{V_{ss}} = 1.61 \text{ vac.}$

(ii) With variables independent, $\sigma_{V_{ss}} = 2.29 \text{ vac.}$

Correlations thus affect the result giving smaller variations than with assumed independence.

The above results are not as pessimistic as those obtained with end-limit calculations earlier; however, evaluation of contributions of individual terms in Equation (20) to output voltage standard deviation would not provide any additional information of utility for identifying sources of variation. For further calculations, the major use of the moments method was to investigate the effects of voltage regulation loop gain on output voltage variations.

The concept of optimizing loop gain to minimize output voltage variations was introduced earlier and the criterion specified was to select the gain which minimizes the mean square deviation from nominal (or equivalently the standard deviation). Using half-load conditions, standard deviations were computed for the four values of N_f and the results are summarized in Figure 13. For both plots shown, the standard deviation of input voltage was 1.125 vdc so that the 4σ value (assumed to represent absolute maximum variation) represents ΔV_{in} giving a 23.5 to 32.5 vdc range. For the upper plot, all other Δx_1 values in Table XI were specified as 4σ values. These results show that increased loop gain, by providing some positive feedback, does decrease output voltage variations as described; however, the minimum variation occurs for $N_f = 1$. Since these results are affected by the magnitude of the circuit parameter variations assumed, the calculations were performed also by reducing all variations by one-half except for input voltage variation. These results are similar

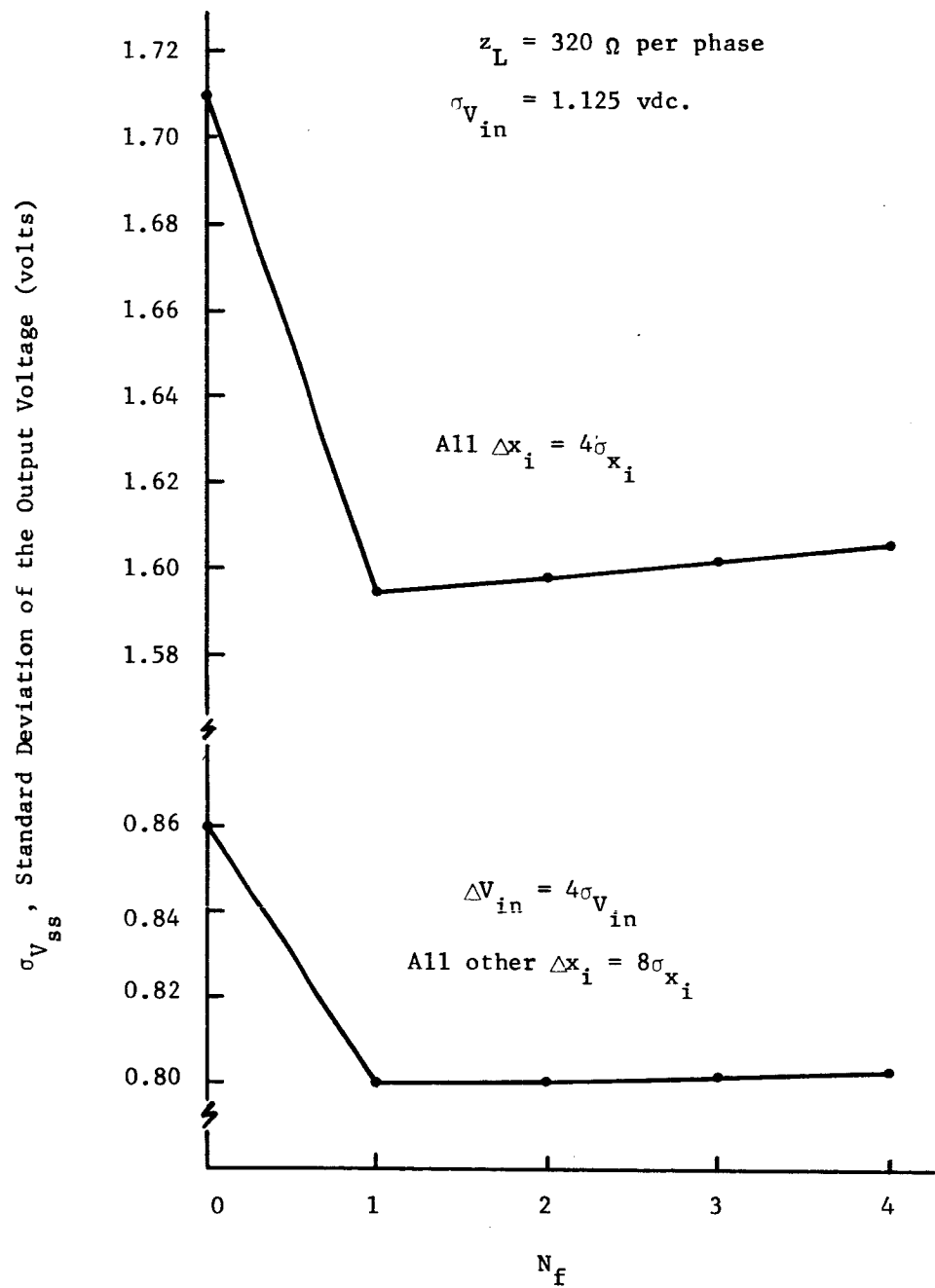


Figure 13. Output Voltage Variation as a Function of Magnetic Amplifier Gain Parameter, N_f

with the minimum but not as pronounced and still occurring at $N_f = 1$. As a reminder, the sensitivities of output voltage to individual circuit parameter variations were introduced with Figure 11 and sensitivity to input voltage decreased with increasing gain as desired. The increase in output voltage with increasing gain, even though small as shown in Figure 13, reflects the combined effect of all variables thus offsetting the reason for using high gain. The use of still smaller variations of circuit parameters while allowing the same variation in input voltage would reverse the results for high gain; however, the variations assumed for the lower plot are considered very realistic.

For either plot in Figure 13, the minimum is not adequately pronounced to declare a specific gain as optimum; however, firm conclusions are drawn with regard to recommended gain. As described in Section 3.3.4.15, some positive feedback in the magnetic amplifier is desirable to speed up its response; however, the design philosophy noted was to achieve the highest magnetic amplifier gain possible with gains near infinity obtained. Based on the above results, nothing is to be gained in terms of output voltage regulation by maximizing the gain. It is also known, and noted in Section 3.3.4.15, that the maximization of the magnetic amplifier gain leads to highly non-linear gain characteristics with the many anomalies introduced not amenable to analytical treatment. Attempts to maximize the gain in breadboard circuitry have led to reverse regulation characteristics for the loop with the output voltage increasing with increasing load (decreasing z_L). This resulted from sign reversals of the magnetic amplifier gain characteristics. Studies described later for transient response of the loop revealed no significant changes in response characteristics with decreases in N_f . Stability of the loop has never been a problem. No other engineering considerations have been noted which might cite the need for providing the extremely high gain of the magnetic amplifier except possibly some experience of the designer which is unknown to the analysts at this time. Engineering confidence can accrue by resorting to a gain that conveniently permits analytical treatment of the loop operation. It is, therefore, recommended that the positive feedback in the magnetic amplifier circuit be limited to an amount which permits it to operate with linear gain characteristics. Any equivalent value between 1 and 3 for N_f is considered adequate and can be obtained by changing the ratio of R67 to R69 instead of the actual value of N_f .

Monte Carlo simulations were conducted to obtain distribution characteristics of output voltage. These analyses involved direct computation of output voltage with the analytical model of Equation (16) for circuit parameter values selected at random from assumed distributions. Since the results did not differ significantly

from those obtained with the moments method, they are not presented herein. The studies are described in Vol. I.

(c) Empirical Studies

Experiments were performed with the inverter breadboard circuit to obtain data for verifying the model for the average three-phase output voltage and for further analysis of its behavior for different inputs, loads and environments. First, an experimental determination of the sensitivities of output voltage to circuit parameter variations was performed by actually changing the circuit parameter values and recording the change in output voltage. Both empirical and analytical values are presented in Table XV for the most significant sensitivities at $N_f = 0, 3, 4$ for full load conditions. In general, agreement is very good. The larger per cent differences exist for the smaller values and were not considered important enough to trace. It is noteworthy that the empirical sensitivity to input voltage variations is greater than the analytical result with the greatest difference at $N_f = 4$. This provides further support to the argument for using less loop gain than that provided for $N_f = 4$.

As further support of the modeling effort performance tests were conducted with the breadboard circuit to measure output voltage for different inputs, loads, and temperature environments.

TABLE XV
Comparison of Empirical and Analytical Sensitivities of Output
Voltage to Circuit Parameter Variations
(Full Load, $z_L = 160 \Omega$ per phase)

Circuit Parameter	Sensitivity					
	Values of N_f					
	0		3		4	
	(Emp.)	(Anal.)	(Emp.)	(Anal.)	(Emp.)	(Anal.)
V_z	0.044	0.048	0.043	0.048	0.044	0.048
R_{73}	-0.042	-0.043	-0.041	-0.043	-0.041	-0.043
R_{75}	0.046	0.046	0.047	0.046	0.047	0.046
R_{74}	-0.00722	-0.0023	-0.00704	-0.0032	-0.00683	-0.0034
V_{in}	0.00422	0.0037	0.00070	0.00086	0.00054	0.00015
V_g	-0.00163	0.0006	0.00011	0.0019	-0.00044	0.0022

The results are summarized in Figures 14 through 25. The first six figures pertain to balanced resistive load conditions and the latter six to balanced inductive loads with a reactive angle of +45 deg. (power factor of 0.707, voltage leading current).

The first group of three figures consecutively show measured performance for fixed ambient temperatures of 100°C(high), 28°C(room), and -25°C(low) with three input voltage conditions of 30 vdc (maximum), 28 vdc (nominal), and 25 vdc (minimum) as given in each figure. Due to differences between the breadboarded circuit and the final packaged form of the circuit such as physical layout, heat sinking, and potting, the exhibited dependence on temperature does not explicitly represent that for the final package but does serve to indicate in a gross manner the effects of temperature on performance. The second group of three figures contains the same information but plotted in a different order, consecutively showing measured performance for the three input voltage levels with the three temperature levels treated parametrically. The last six figures for inductive loads are arranged similarly.

The two sets of data were collected at different times and it is noted that the calibrations, the values of output voltage at half-load, nominal input and room temperature, are slightly different; however, the characteristics of interest are the variations from the preset value. One other noted difference is the low levels for ambient temperature, -25°C for resistive load and -7°C for inductive loads, which resulted from a lack of control in the cooling chamber.

For both loads, variations from the preset values over the full range of load (from no load, to rated load), temperature, and input voltage were within ± 1.0 volt requirement. Thus static regulation capabilities are adequate. The regulation extends well beyond the rated load conditions with the minimum occurring at approximately 1.5 amp line current for a resistive load at high temperature and low input voltage. The overload mode of operation is discussed in Section 3.3.3.3.

With the two sets of data for operation within rated load conditions, i.e., the normal mode, empirical models were obtained for output voltage V as linear combinations of temperature T , input voltage V_{in} , and line current I_B with least squares analysis techniques. These models represent only crude approximations for performance but are helpful for assisting in observing the effects of the independent variables. The models are:

Resistive Load

$$V = 114.077 - 0.00293T + 0.0352 V_{in} - 0.1405 I_B$$

Inductive Load

$$V = 113.74 - 0.00199T + 0.0440 V_{in} - 0.3224 I_B$$

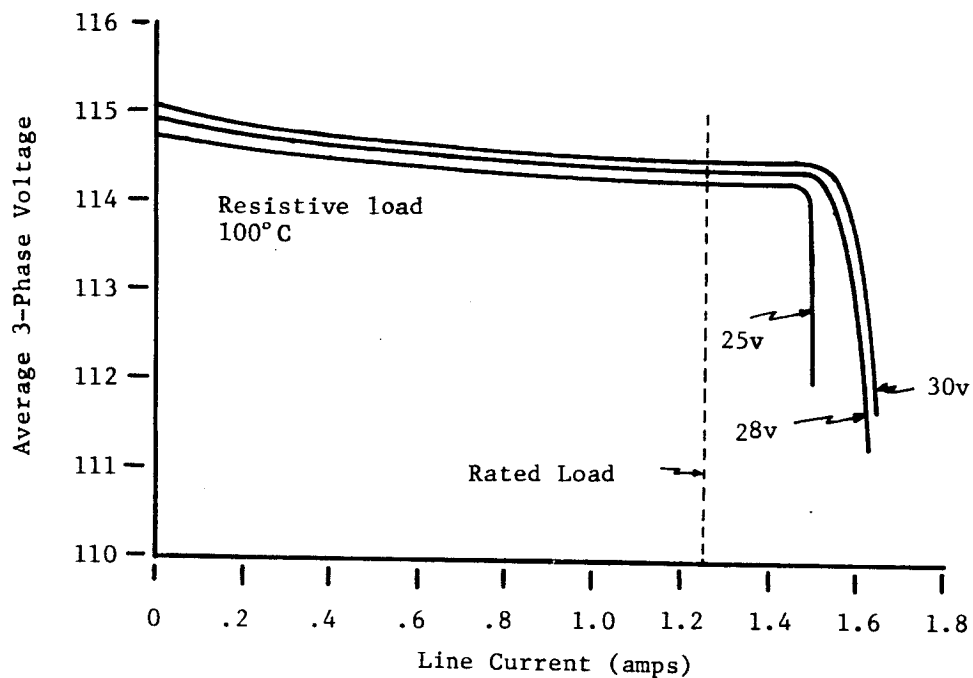


Figure 14. Average 3-Phase Voltage Versus Line Current;
Resistive load; 100°C

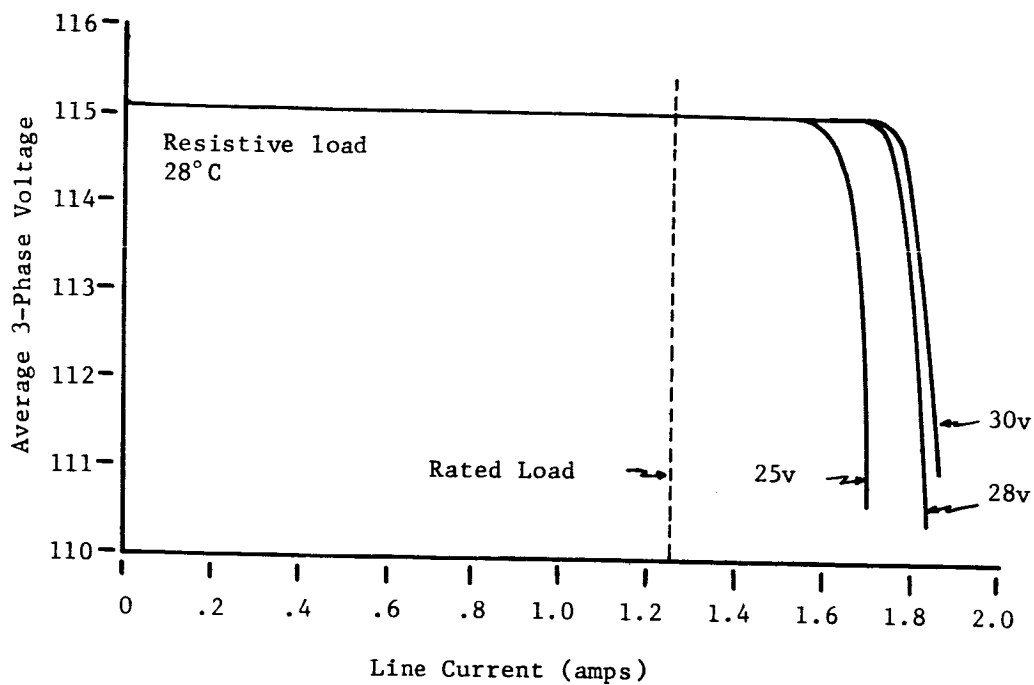


Figure 15. Average 3-Phase Voltage Versus Line Current;
Resistive load; T = 28°C

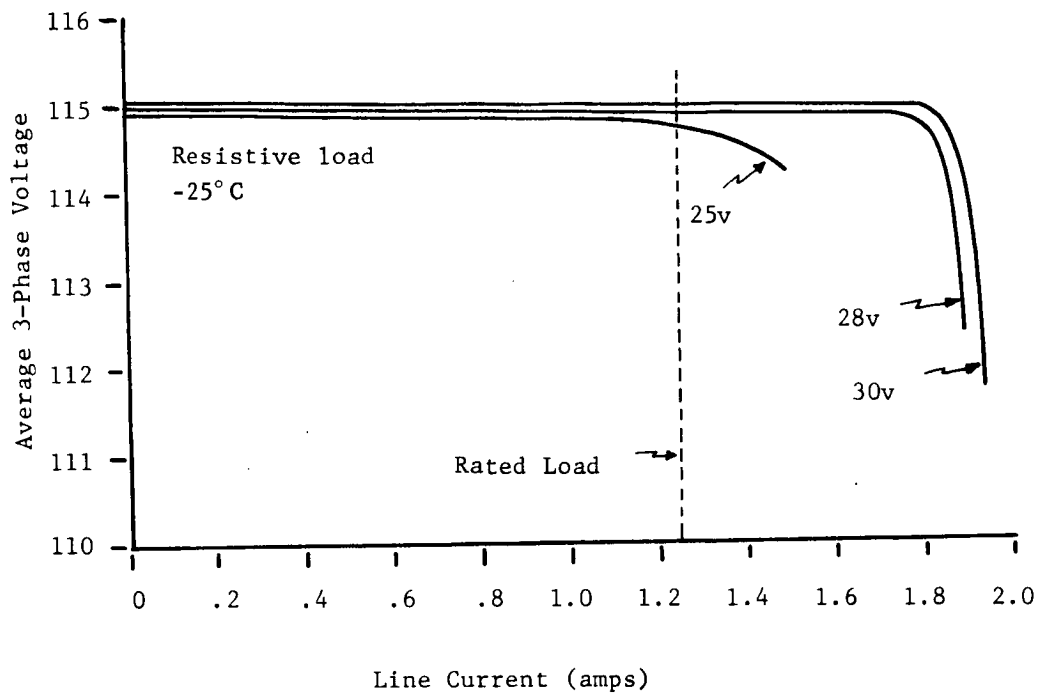


Figure 16. Average 3-Phase Voltage Versus Line Current;
Resistive load; $T = -25^{\circ}\text{C}$

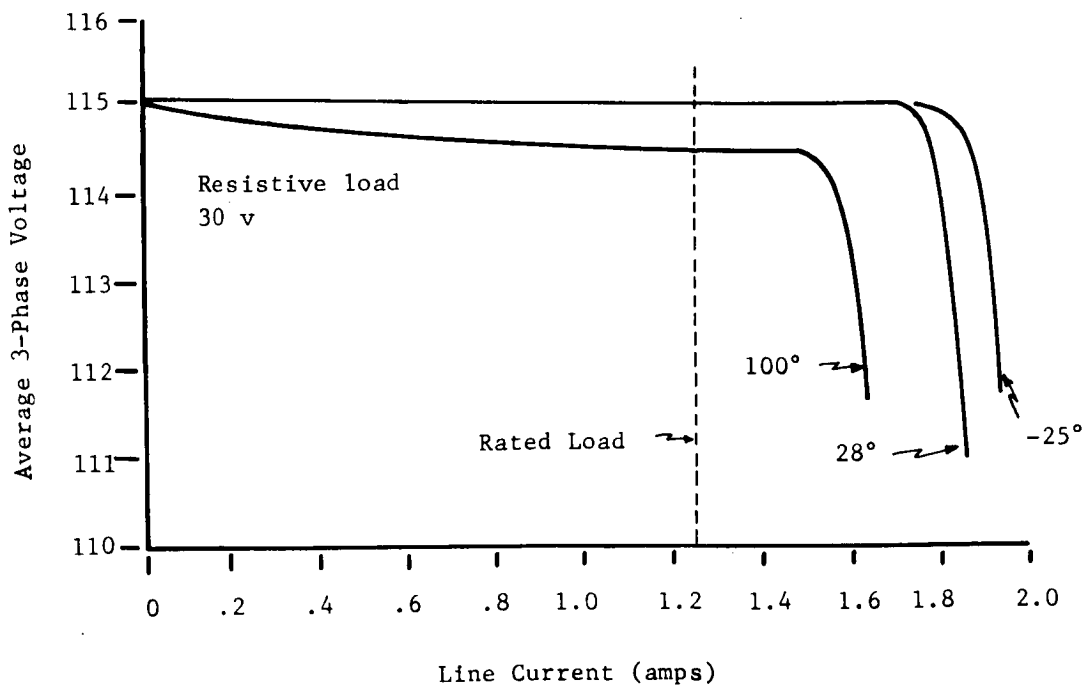


Figure 17. Average 3-Phase Voltage Versus Line Current;
Resistive load; $V_{in} = 30\text{V}$

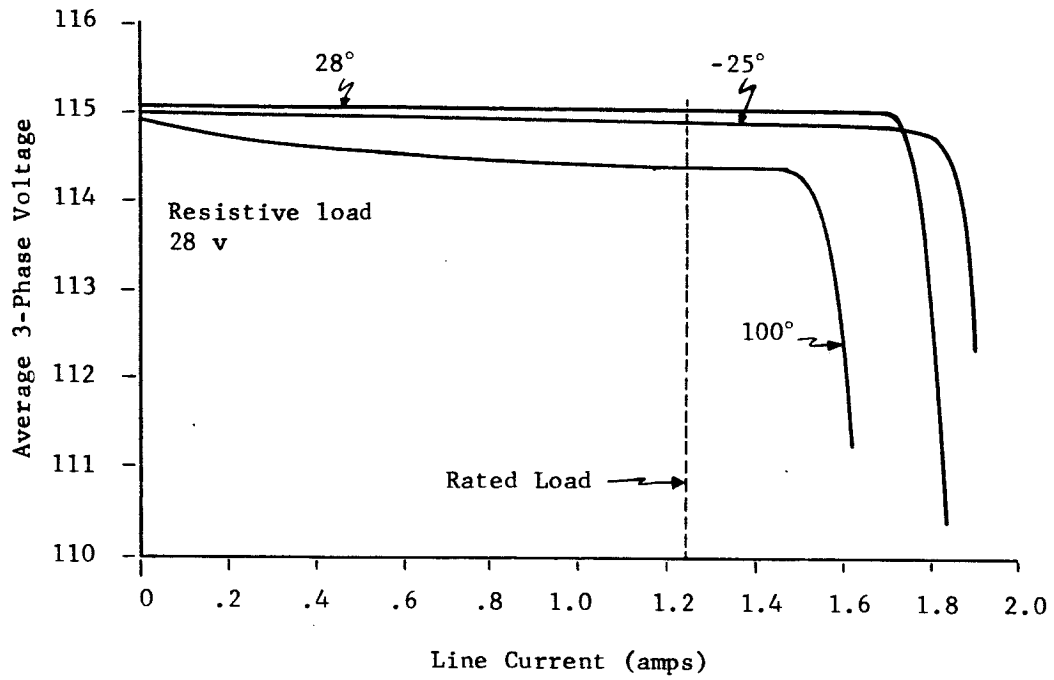


Figure 18. Average 3-Phase Voltage Versus Line Current;
Resistive load; $V_{in} = 28$ v

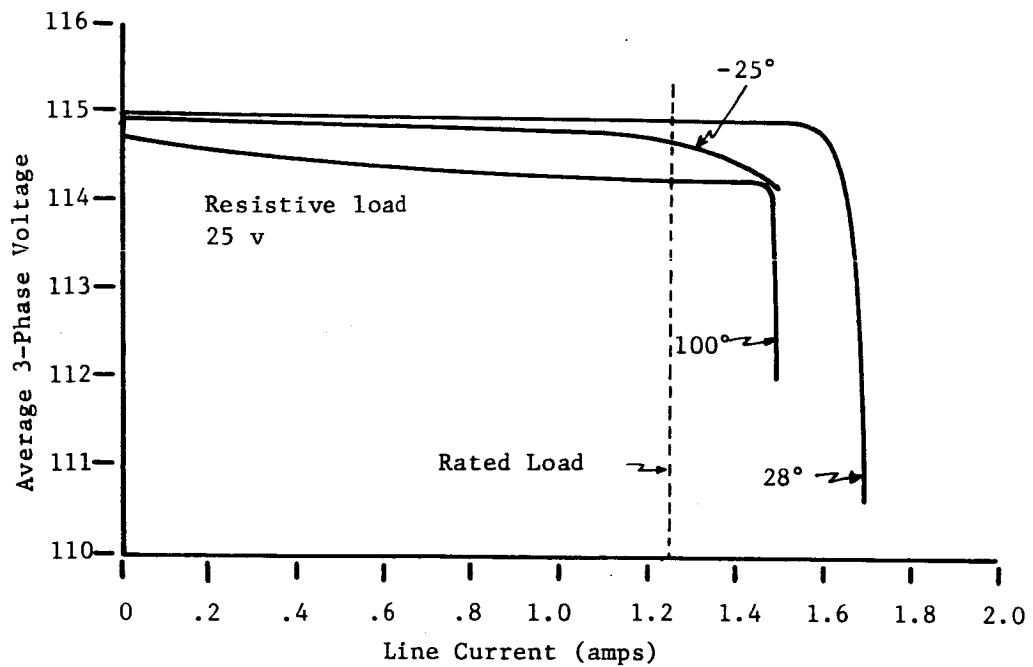


Figure 19. Average 3-Phase Voltage Versus Line Current;
Resistive load; $V_{in} = 25$ v

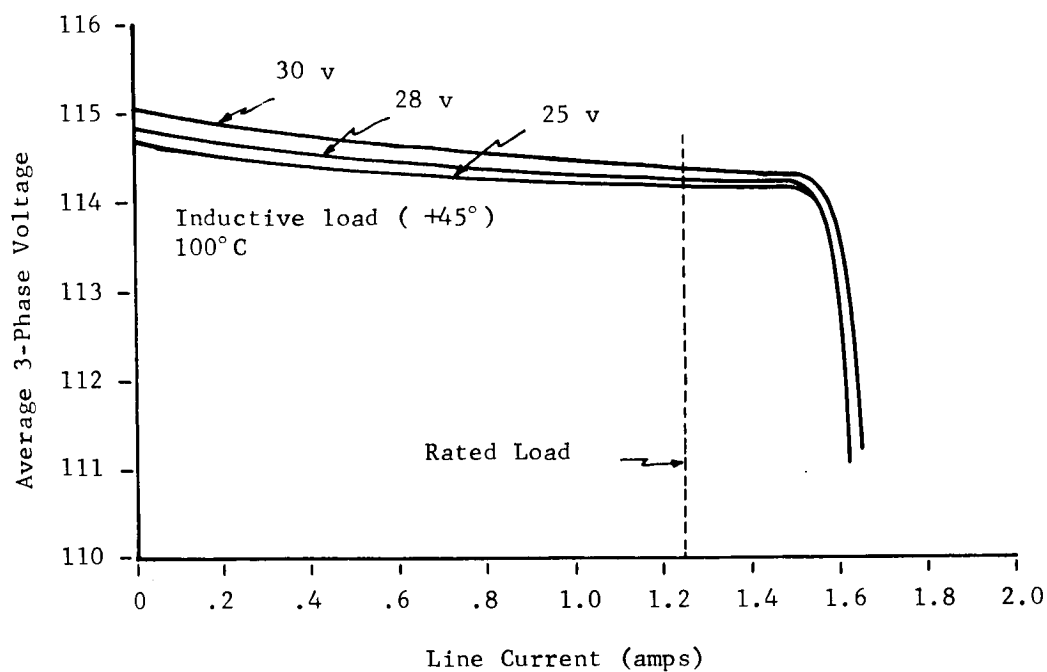


Figure 20. Average 3-Phase Voltage Versus Line Current;
Inductive load (+45°); T = 100°C

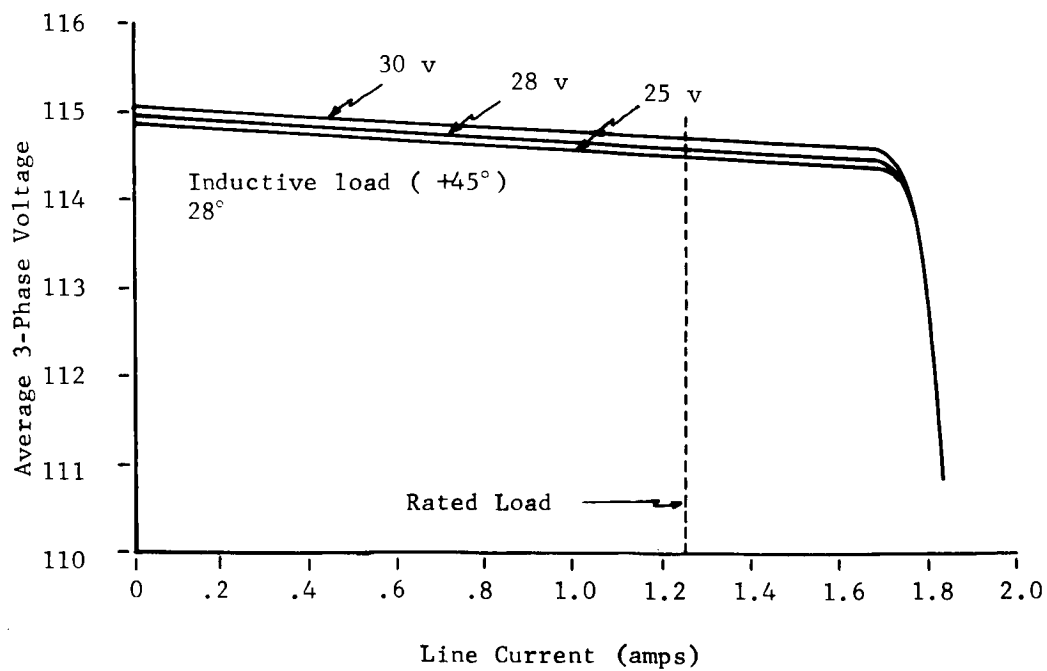


Figure 21. Average 3-Phase Voltage Versus Line Current;
Inductive load (+45°); T = 28°C

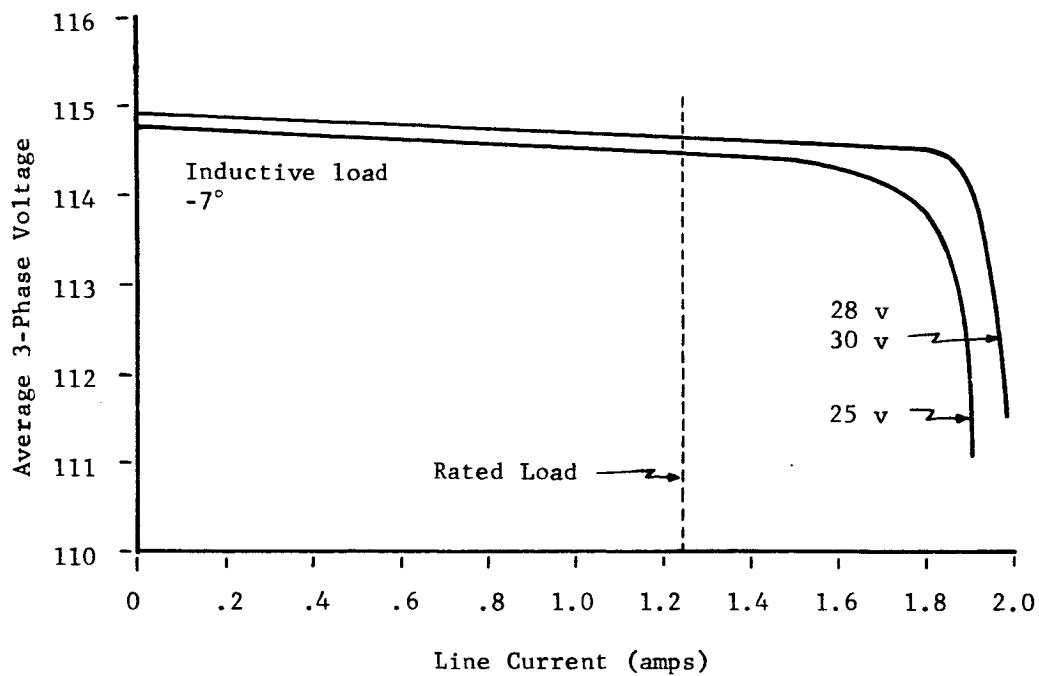


Figure 22. Average 3-Phase Voltage Versus Line Current;
Inductive load ($+45^\circ$); $T = -7^\circ\text{C}$

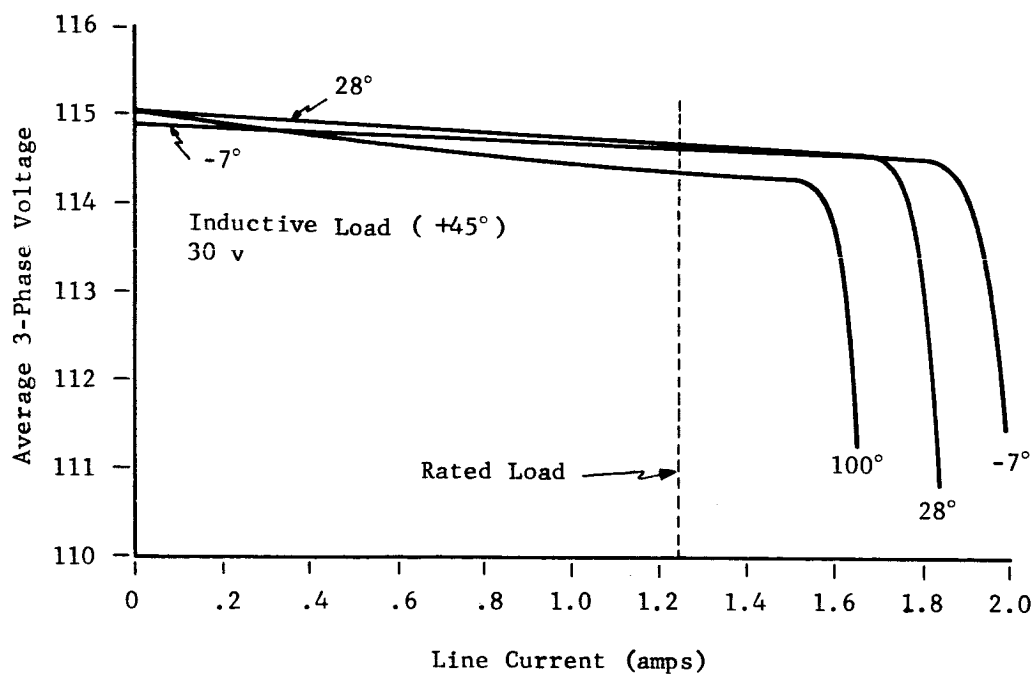


Figure 23. Average 3-Phase Voltage Versus Line Current;
Inductive Load; $V_{in} = 30\text{ v}$

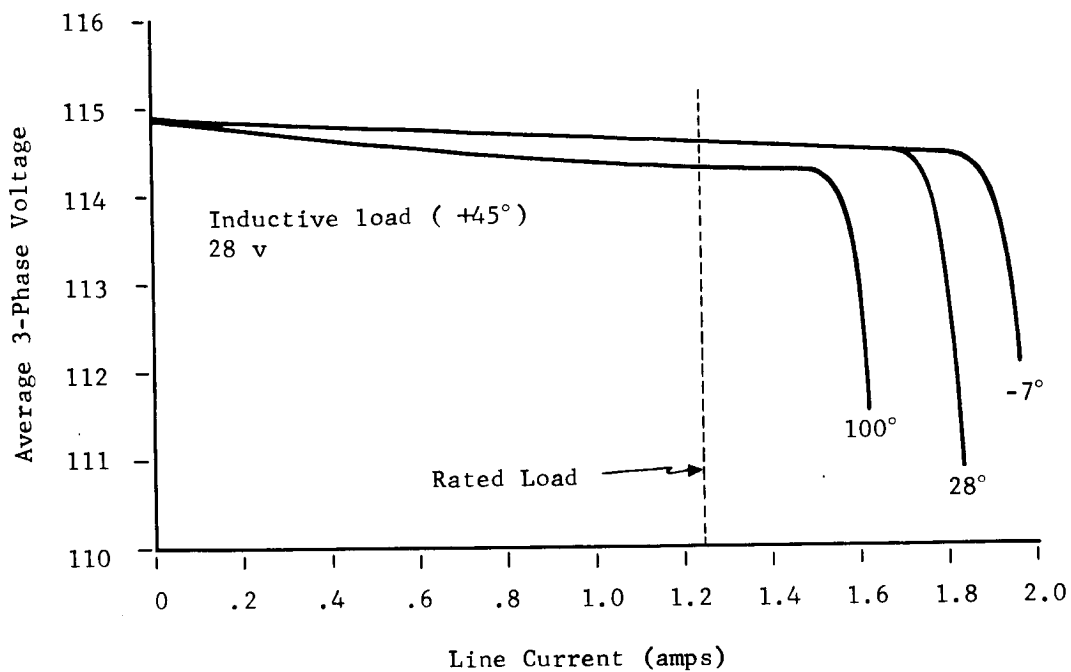


Figure 24. Average 3-Phase Voltage Versus Line Current;
Inductive load (+45°); $V_{in} = 28$ v

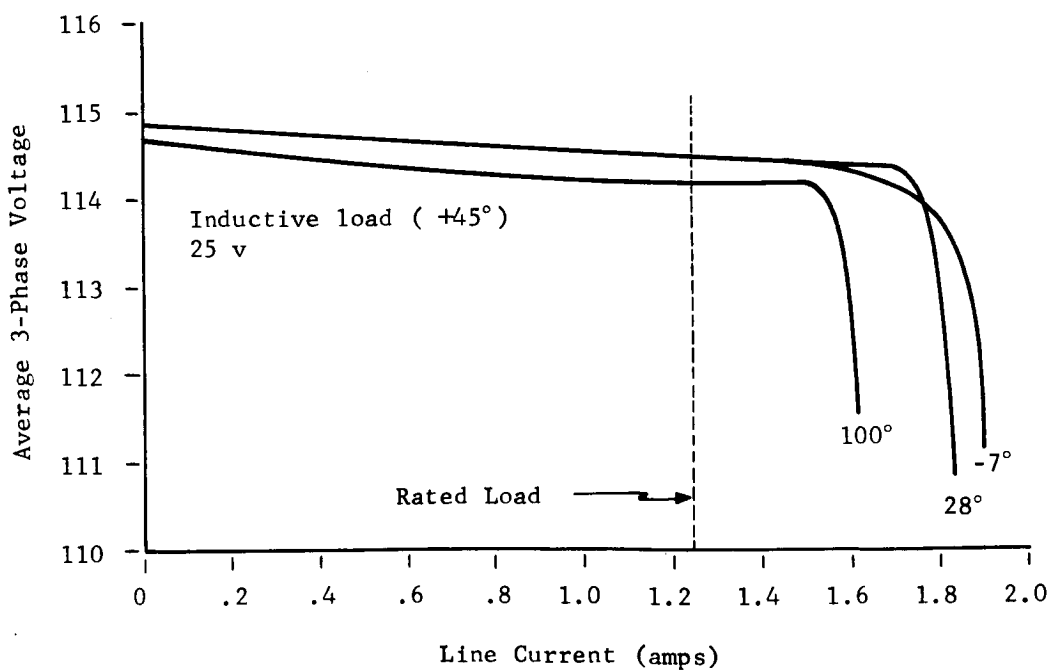


Figure 25. Average 3-Phase Voltage Versus Line Current;
Inductive load (+45°); $V_{in} = 25$ v

It is first noted that the models differ in form from the regression models presented in earlier analyses in that the absolute values, instead of variations about the nominal value, are used. The first terms thus represent the intercept on the V axis and not the mean value.

As indicated by the signs of the coefficients, the effects of the independent variables are similar for both resistive and inductive load and differ only in magnitude. The temperature coefficients indicate decreasing output voltage with increasing temperature with a stronger dependence for resistive loads. This is evident in the data for high temperatures; however, at low temperatures, it is obviously less with even a reversal indicated. A more elaborate model for representing the changing dependence would involve higher order terms, but the effort for obtaining it is not justified.

The effect of input voltage variations is larger for inductive loads with increases causing an increase in output voltage. This is anticipated from the nature of the voltage regulation loop operation. Comparison with the data shows agreement, with the largest effect occurring at high temperature.

With respect to the size of the load, the models indicate considerably stronger dependence for inductive loads, with output voltage decreasing with increased load (or line current). This effect is shown in the curves with the dependence strongest at high temperatures.

These considerations indicate that high ambient temperatures have a pronounced effect on output voltage variations. Even though regulation capability is adequate, some improvement could be achieved by controlling the ambient temperatures. An alternate possibility is to obtain thermal equilibrium before manually adjusting the output voltage.

(2) Transient Response Mode

The attributes selected to describe the loop transient response are the maximum output voltage deviation during a transient, ΔV_{tr} , and the transient time, t_{tr} . The simultaneous equations, Equations (12) and (13), were presented earlier in this section to describe the transient response of the voltage regulation loop. Each equation is linear in the response to its particular forcing function; however, the system described by both is non-linear due to the product term $V_{in} \tau$. Because of the potential difficulty in experimentally measuring the transient characteristics, it was especially desirable to use an analytical approach with Equations (12) and (13) providing the basic analytical description. Due to complexity of the equations, a direct closed form solution for the two attributes of interest is not feasible. The approach selected is described by sequential steps as follows:

- (a) Define analytical models for each of the coefficients A_0 , A_1 , B_0 , B_1 , C_1 , C_2 , and k with the functional relationships in Appendix B.
- (b) Using end-limit techniques as described in (1) above, determine ranges of variation of the coefficients.
- (c) With Equations (12) and (13) perform analog computer simulations of the loop transient response for the variations of the coefficients as determined in (b).
- (d) Formulate regression models for maximum voltage deviation and transient time using the results of (c).
- (e) Use the regression models to analyze for attribute behavior.

Results of the above approach were unsatisfactory, as evidenced by the inability to obtain a stable loop in (c) for nominal values of the independent variables. This, of course, implies that Equations (12) and (13) do not provide an adequate description of the loop transient response. Since success was achieved with the steady-state solution, the models for the coefficients A_0 , A_1 , and k were the chief suspect for discrepancy. (Even though A_0 and k appear explicitly in the steady-state model defined by Equation (14), the independent variables involved disappear by cancellation when their expressions in Appendix B are substituted.) Attempts were made to evaluate these coefficients experimentally with the breadboard circuit. As described in Section 3.3.4.15, some degree of success was achieved for k . Similar attempts for A_0 and A_1 described in Section 3.3.4.16 led to the discovery that the transient response of the forward portion of the loop was highly non-linear, invalidating Equation (13). Further measurements established that the non-linearity existed in the output filter portion of the primary voltage regulator circuit. The initial assumptions made in the derivation of Equations (12) and (13) for linearizing the response of this circuit thus proved to be invalid. The complex non-linear characteristic could not be feasibly determined experimentally thus precluding the ability to use the approach outlined above. Even though difficult, the remaining course was to experimentally observe the transient attributes.

For response to input voltage disturbances, initial experiments consisted of stepping the input voltage 0.75 v from 29.0 v to 29.75 v with the inverter loaded with 475 Ω per phase (0.42 amps line current) and observing the transients in the output voltage waveform without regard to the time at which the disturbance was introduced. The observed transient time t_{tr} was consistently less than 40 msec, while the maximum voltage deviation ΔV_{tr} was unpredictable ranging in magnitude from -50 v to +30 v.

Instrumentation was then provided to control the time during the inverter 400 cps fundamental period at which the disturbance was introduced. A reference signal for switching the disturbance was derived from a flip-flop output in the

active timing generator with a manually set delay used to control the relative switching time. The observed ΔV_{tr} for one phase of the output is plotted in Figure 26 as a function of the controlled delay time θ with the range of θ covering the equivalent of $2 \frac{1}{2}$ times the 2.5 msec. period of the 400 cps. Even though resolution is not fine, a distinct periodicity of ΔV_{tr} of 2.5 msec. is obvious revealing the anticipated dependence on time of disturbance. Similar curves for the other two phases would reflect the same type of relationship. Shorter period oscillations reveal some semblance of periodicity but were not resolved. By detailed analysis, these could be related to operation of the voltage error detection circuit and the 2400 cps ripple obtained in detecting the output voltage.

A typical response is illustrated in Figure 27 showing both the input disturbance and the output transient. The input disturbance was provided by shunting out a resistor in the source bus. The oscillations in the input voltage are due to combined affects of the inverter input filter and the source impedance, but no attempt was made to describe these characteristics in detail. Some of the rapid oscillations in the output waveform are interpreted as responses to the input oscillations; however, the input disturbance shown was considered to adequately represent a step input. The 5% requirement stated for ΔV_{tr} is interpreted as 5% of peak voltage or 8 v. The major result of interest interpreted from Figure 27 is that transients significantly larger than 8 v are possible; however, since disturbances during application will occur at random, the liklihood of large transients is small. For given conditions, this liklihood is simply equivalent to the liklihood that the disturbance occurs during a critical interval in which $|\Delta V_{tr}|$ exceeds 8 v. Specifically, for the conditions employed in the test

$$\text{Prob } \{\Delta V_{tr} > 8 \text{ v}\} \approx 0.36, \quad (19)$$

where the probability is estimated as the relative time that θ lies in the critical intervals, the disturbing time is assumed uniformly distributed over the 2.5 msec. period, and a multiple factor of these is used to account for the other two phases.

The probability is, in general, dependent upon the type and size of disturbances; other conditions such as load level, temperature, and input voltage at the time of disturbance; and values of significant circuit parameters. The major types of disturbances considered of interest are step changes in load and spurious short term transients on the input. A complete analysis would involve obtaining curves as in Figure 26 for different values of the many factors identified. From the observed results, regression models could be formulated for the attribute behavior as functions of the independent factors. Due to limitations on available effort, extensive investigations were not performed. Some further effort described below was devoted to

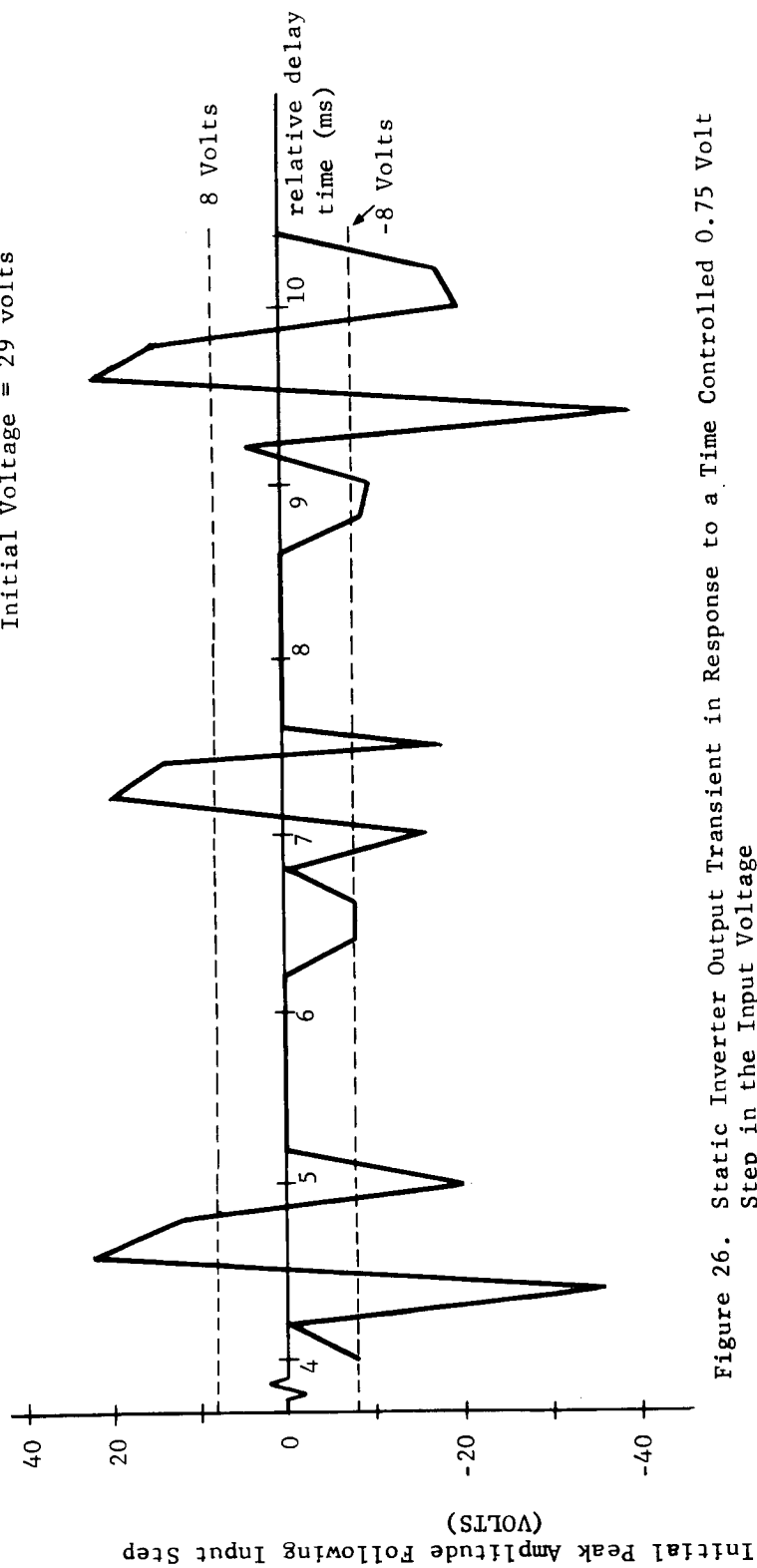
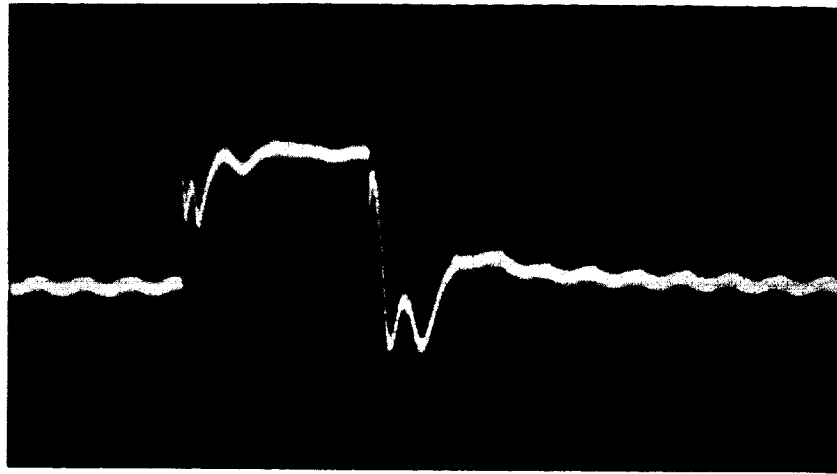


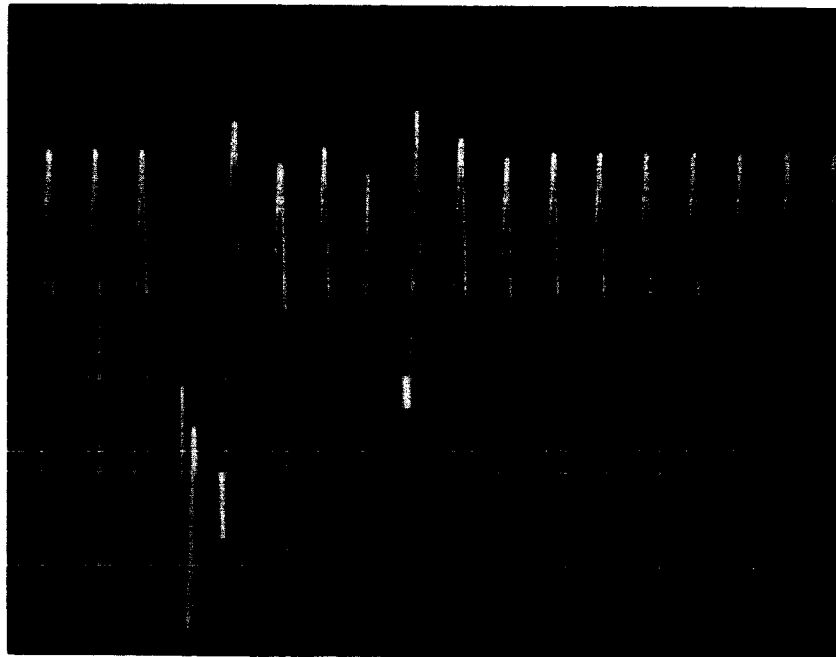
Figure 26. Static Inverter Output Transient in Response to a Time Controlled 0.75 Volt Step in the Input Voltage



Input Disturbance

Vertical Scale: 2 V per div.

Horizontal Scale: 5 msec. per div.



Output Transient

Vertical Scale: 20 V per div.

Horizontal Scale: 5 msec. per div.

Figure 27. Typical Output Response to Input Disturbance

additional study of the response to step changes in input voltage. Turn-on and turn-off transients are treated separately below. A transient originating internally due to switching of a redundant timing generator is also extended brief consideration below under this heading. Responses to short-term spurious input transients and step changes in load were not explored; however, from the experience with responses to the other disturbances the nature of the response is expected to be similar.

For further study of response to steps in input voltage, the value of θ in Figure 26 that produced the largest ΔV_{tr} , viz 9.4 msec., was selected for investigation of circuit parameter variations and other conditions. Circuit parameters V_Z , R_{73} , R_{75} , L_R , C_R , and $k = R_e/K'_\phi$, itself, were selected as the most likely parameters for which variations would affect the transient response. k represents the inverse of the magnetic amplifier rise time and was effectively varied by changing N_f from its nominal value of 3 turns to 2 turns and 4 turns to collectively account for parameters K_ϕ , R_{67} , R_{69} , N_f , and R'_g . The parameters defined above were varied one-at-a-time by amounts listed in Table XI and ΔV_{tr} observed for the 0.75 step in input voltage from 29.0 v to 29.75 v and 475 Ω per phase inverter load. No significant changes in the output voltage transient were observed for any changes in circuit parameters.

Some observed results for several other conditions of input voltage, load, and step size are presented in Table XVI. The data is sparse because of limited effort but serves to illustrate the highly non-linear character of the loop operation during transients. With the data in Table XVI a simple linear regression model for ΔV_{tr} was obtained as

$$|\Delta V_{tr}| = -2.248 + 1.432 V_{in} - 12.06 I_{out} + 7.689 \Delta V_{in}; \quad (20)$$

however, this expression is not an accurate description of the behavior of ΔV_{tr} and its major utility is the separation of the effect of the individual variables for determining the direction of influence. For example, ΔV_{tr} is shown to increase with increasing step sizes ΔV_{in} as anticipated while the effect of increased load (line current, I_L) is to decrease ΔV_{tr} . With more data, a more accurate model could be formulated and would of necessity include higher degree terms to account for non-linear effects such as the known non-linear dependence on ΔV_{in} .

Consideration of transients caused by switching from one redundant timing generator to the other was limited to observing a number of responses at different inverter load conditions. No attempt was made to control the time at which the switching occurred; however, for a number of sequential observations at fixed loads, the transients appeared to be very similar. Typical transients for the extremes of no load and full load are presented in Figure 28. During the switch-over, the out-

TABLE XVI

Summary of Results for Measurements of
Transient Response to Step Disturbances in Input Voltage

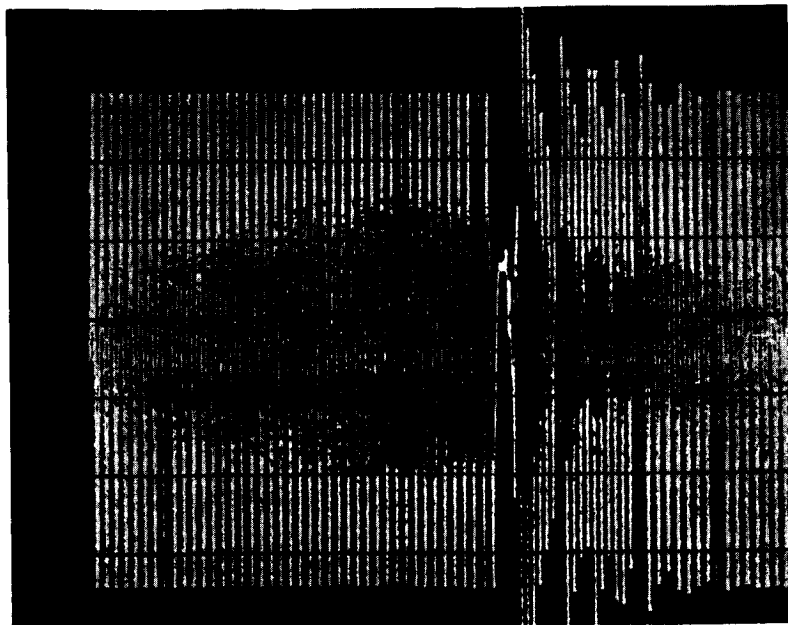
Input Voltage V_{in} (volts)	Line Current I_{out} (amps.)	Step Size ΔV_{in} (volts)	Output Voltage Maximum Deviation ΔV_{tr} (volts)
29.0	0.42	0.75	-40
26.6	0.60	2.8	-50
30.0	0.60	2.8	-55
24.0	1.2	5.5	-60
30.0	0	0.55	-45

put essentially disappears for about three cycles and then resumes operation. The maximum voltage deviation thus greatly exceeds the typical requirements of 5%. The damped oscillations in the waveform envelope during the restart are dependent on load with decreased amplitude and increased damping occurring with increased load. The switchover process is further complicated by the initial states of the activated flip-flops in the pulse sequence generator and the timing pulse amplifier stages that follow.

A startling effect apparent in the oscillograms in Figure 28 is a distinct increase in frequency just following the restart, continuing for several cycles, and then returning abruptly to the normal frequency. Time has not permitted fully resolving the cause; however, observations on the primary oscillator output identifies the crystal as the source. In the no load transient of Figure 28, the frequency increase is 50% to 600 cps for a duration of 17 cycles, while in the full load transient, the increase is to 525 cps for a duration of 11 cycles. The same effect is apparent in the turn-on transient which is shown in Figure 29 and discussed below, with a frequency of 480 cps present for a duration of 10 cycles. The potential seriousness of this effect has not been assessed but is dependent on the inverter application. Some further discussion on this effect is presented in Section 3.3.4.3.

(3) Turn-on and Turn-off Modes

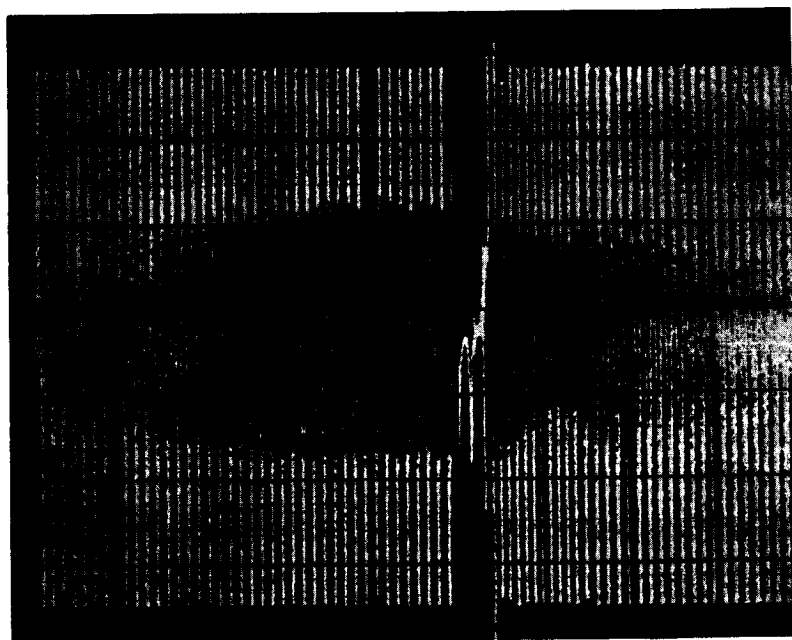
Major attributes of interest during these modes were voltage overshoot during turn-on and turn-off times. Consideration was limited to observing transients for



No Load

Vertical Scale: 50 V per div.

Horizontal Scale: 20 msec. per div.

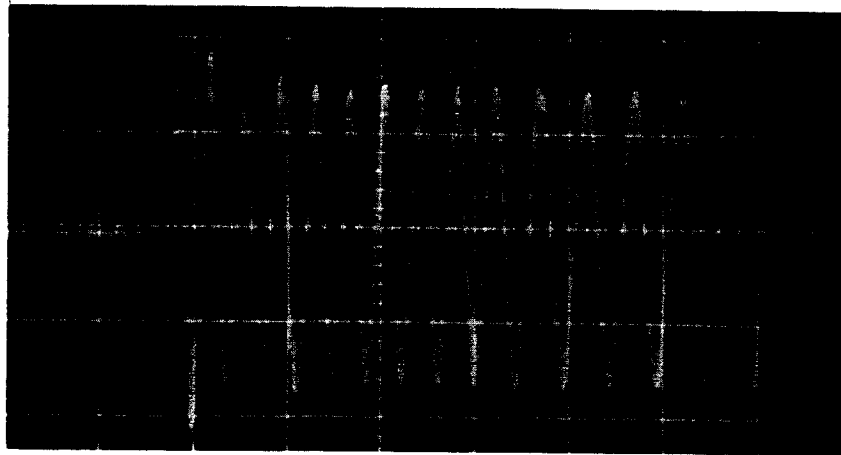


Full Load

Vertical Scale: 50 V per div.

Horizontal Scale: 20 msec. per div.

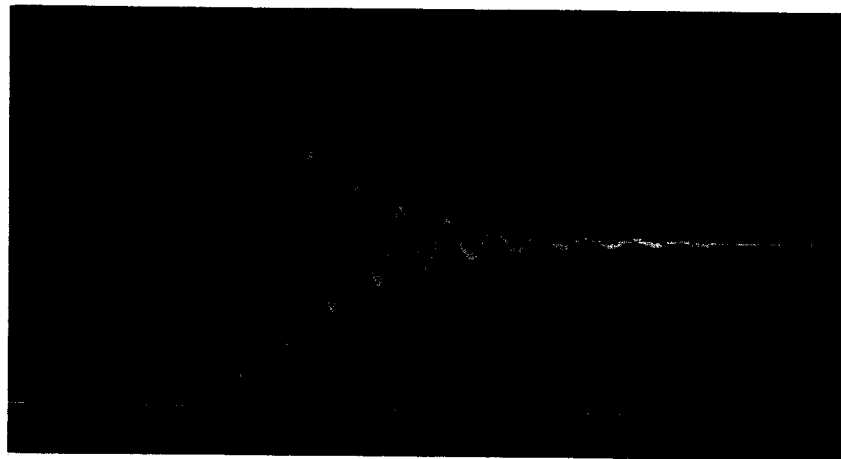
Figure 28. Typical Output Transients for Switching from One Redundant Timing Generator to the Others



Turn-on

Vertical Scale: 100 V per div.

Horizontal Scale: 5 msec. per div.



Turn-off

Vertical Scale: 100 V per div.

Horizontal Scale: 5 msec. per div.

Figure 29. Typical Output Voltage Transients During Turn-on and Turn-off

an input voltage of 30 vdc and half-load conditions ($I_{out} = 0.6$ amp.). Typical transients are shown in Figure 29. Both turn-off and turn-on occur within 20 msec. Voltage over-shoot during turn-on is approximately 40 v or about 25% of the peak voltage thus exceeding the 15% stated requirement. From the transient response analysis described above, this can be expected to improve with increased load and lower input voltage.

3.3.3.3 Overcurrent Protection Loop (Element 19)

This section presents a brief analysis of the static inverter overcurrent protection (OCP) loop. Its purpose is to limit output voltage and current of the inverter during the overload mode of operation. The OCP loop operates in parallel with the voltage control loop as shown by the functional diagram in Figure 10, but is active only during excess output current demands. The static and dynamic characteristics of the OCP loop are similar to those of the voltage control loop, and maximum use is made of the analysis of the voltage control feedback loop.

An analysis of the voltage control loop was presented in Section 3.3.3.2. The equation,

$$\frac{d\tau}{dt} + \frac{R_e}{K'_\phi} \tau = C_1 + C_2 V, \quad (21)$$

was used to describe the feedback portion which included the voltage error detection circuit and the magnetic amplifier. In deriving this equation, those terms representing the overcurrent control winding were neglected. If the derivation is repeated including the overcurrent control winding terms, Equation (21) becomes

$$\frac{d\tau}{dt} + \frac{R_e}{K'_\phi} \tau = C_1 + C_2 V + \frac{R_e N_g N_{c2}}{V_g R_{c2}} V_{c2}, \quad (22)$$

where N_{c2} is the number of turns in the overcurrent control winding and V_{c2} and R_{c2} are the source voltage and impedance of a Thevenin's equivalent for the drive circuit, i.e., the overcurrent detection circuit. The other parameters have been previously defined. V_{c2}/R_{c2} is the control current in the overcurrent control winding, I_{c2} . The overcurrent protection loop has no effect on the analytical description of the forward portion of the loop, and that by determining the relationship between output line current I_L and I_{c2} , Equation (22) will provide for a static and dynamic description of the static inverter in the overcurrent mode of operation. A linear magnetic amplifier transfer characteristic was assumed to derive Equation

(21), however, and will be valid only while the magnetic amplifier is operating in its linear region.

To examine the relationship between I_L and I_{c2} , reference is made to the over-current detection circuits (ODC) of Figure 51. The steady-state relationship is considered initially, and a consideration of transient conditions will follow. It was shown that the three-phase rectifier voltage in the ODC was 6.05 volts per rms ampere of output line current. Consequently, for the ODC circuit, the equations describing the operation are

$$\frac{6.05 I_L - V_{Z2} - V_{BE} - (I_{c2} + I_B) R_{60}}{R_{61}} = I_{R29} + I_B,$$

$$I_{R29} = \frac{V_{BE}}{R_{29}},$$

$$I_{c2} = h_{FE} I_B, \text{ and} \quad (23)$$

$$I_B = \frac{V_{BE} - V_1}{R_{BE}};$$

where V_{Z2} = the zener voltage of CR148,

V_{BE} = Q35 base-emitter voltage,

I_B = Q35 base current,

h_{FE} = Q35 dc gain, and

V_1 and R_{BE} are Q35 base-emitter characteristics defined in Figure 30.

From Equation (23), it can readily be determined that

$$I_{c2} = C_3 I_L + C_4 \quad (24)$$

where

$$C_3 = \frac{6.05 h_{FE} R_{29}}{[R_{BE} + (1 + h_{FE}) R_{60}] R_{29} + (R_{BE} + R_{29}) R_{61}}, \text{ and}$$

$$C_4 = \frac{h_{FE} (V_1 R_{29} - V_1 R_{61} - V_{Z2} R_{29})}{[R_{BE} + (1 + h_{FE}) R_{60}] R_{29} + (R_{BE} + R_{29}) R_{61}}.$$

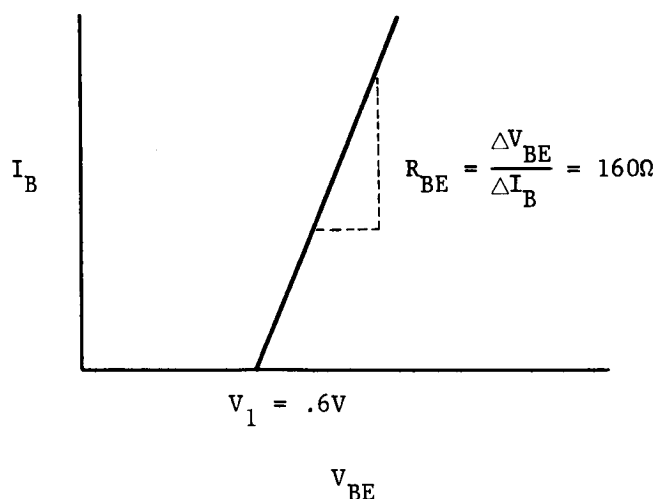


Figure 30. Assumed Q35 Base-Emitter Characteristics.

Assuming that $h_{FE} = 20$, $V_1 = 0.6$ V and $R_{BE} = 160 \Omega$, (h_{FE} is a specified minimum in the region of V_1 and R_{BE} are measured values) Equation (24) evaluates to

$$I_{c2} = (5.54 I_L - 7.5) 10^{-3} \text{ amperes.}$$

Since I_{c2} can not be negative, this is valid for $I_L \geq 1.35$ amps. For $I_L < 1.35$ amps, $I_{c2} = 0$. It is interesting to note that the threshold value for I_L evaluates to approximately the value quoted in Section 3.3.4.12.

Substituting I_{c2} from Equation (24) for V_{c2}/R_{c2} in Equation (22), yields

$$\frac{d\tau}{dt} + \frac{R_e}{K'_{\phi}} \tau = C_1 + C_2 V + \frac{R_{eN} N_{c2}}{V_g} (C_3 I_L + C_4). \quad (25)$$

It is emphasized again that Equation (25) is valid only when $I_L \geq C_4/C_3$. If $I_L < C_4/C_3$, Equation (25) reduces to Equation (22). For the region in which Equation (25) is valid, it can be rewritten as

$$\frac{d\tau}{dt} + \frac{R_e}{K_\phi} \tau = C_5 + C_2 V + C_6 I_L \quad (26)$$

where

$$C_5 = C_1 + \frac{R_e N N c_2}{V_g} C_4, \text{ and}$$

$$C_6 = \frac{R_e N N c_2}{V_g} C_3.$$

Equation (26) is a valid steady-state description of the combined feedback loops. It is also valid for transient conditions in which I_L is increasing since the time constant for C4 in Figure 51 will be small because of the low equivalent source impedance of T11 - T13 and CR105 - CR110. For I_L decreasing, however, an additional first order lag is introduced due to C8 discharging through a minimum of 33 ms which is large with respect to K'_ϕ/R_e . No additional consideration has been given a transient solution, however. Q35 is operating in a region in which h_{FE} changes rapidly with I_{c2} and it would be difficult to obtain accurate transient solutions without an extensive computer program. It is also probable that the magnetic amplifier will not operate in a linear region of its transfer characteristics with the static inverter in an overcurrent mode of operation.

3.3.4 Analyses for Small Circuits

In the following sections, a brief summary of the analysis of each element of the static inverter is presented. Generally, only the conclusions of the analyses are presented. A functional description of each element and its interconnection with other elements was presented in Reference 1 and will not be repeated. A preliminary design analysis of each element has been presented in Reference 2. Those analyses were presented in detail, and generally were a worst-case, i.e., worst-case inputs were assumed, but nominal or measured component parameter values were frequently used in the absence of component characteristic data. As meaningful component characteristic data became available, the analyses of Reference 2 were repeated for actual worst-case conditions, but only in those cases in which the results or conclusions changed significantly will any details be included in this section. The component stress analysis in Section 3.3.1.3 reflect the results of the latest element analyses with respect to component applications.

3.3.4.1 Six-volt dc Regulated Supply

3.3.4.1.1 Original Version (Element 21)

Schematic: Figure 31.

Function: Provide regulated B+ voltage to the elements of the timing generators via the electronic switch.

Input: 25 - 30 vdc (inverter input).

Load: 65 ma computed in Reference 2.

Attributes: (1) Output voltage.

(2) Output voltage ripple.

Remarks: In the preliminary design analysis of Reference 2, it was concluded that the redundancy scheme used in this circuit resulted in the dissipation of more power than was necessary and it was suggested that the circuit function could be performed with fewer parts and increased efficiency. The suggested circuit also eliminated a critical failure mode, the open circuit failure of CR145 or CR146. The design has since been modified, however, such that a non-redundant six-volt supply is included in each of the redundant timing generators. The modified circuit is shown in Figure 32 and discussed in Section 3.3.4.1.2.

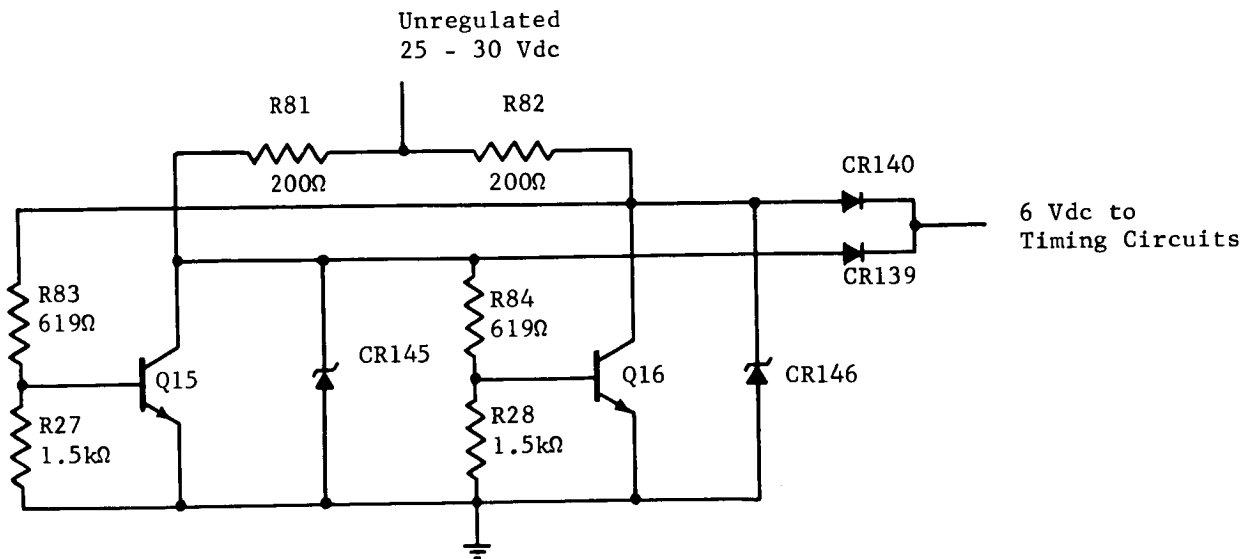


Figure 31. Regulated Six-volt dc Supply (Original Version)

The design of this circuit is concluded to be adequate. It will function as a low impedance, zener source for all expected conditions, and the output voltage will be between 6.2 and 7.5 vdc. The internal power dissipation is not excessive in view of the limiting efficiency of 20% ($6/30 \times 100\%$), and all components are well within their rated capabilities. The output voltage ripple is negligible.

At room temperature, the six-volt supply has been observed to draw 263 ma at 30 volts from the primary voltage supply and supply 63.8 ma at 7.25 volts to the electronic switch. These correspond to an input of 7.9 watts, an output of 463 mw, and an efficiency of 5.9%. The output voltage has been observed to change approximately 4% over the temperature range of interest. No effort was made to select a zener diode with any particular temperature characteristics for the six-volt reference.

3.3.4.1.2 Modified Version (Elements 21M-1 and 21M-2)

Schematic: Element 21M-1 is shown in Figure 32. Element 21M-2 is identical.

Function: Provide regulated B+ voltage to the timing generator elements.

Input: 24 - 30 vdc derived from the inverter input via the electronic switches (modified version).

Load: 145 ma max. This current requirement is significantly greater than that stated for the original version in Section 3.2.4.1.1 and represents the maximum anticipated load requirements of a modified version of the timing generators being considered.

Attributes: (1) Output voltage.
(2) Output voltage ripple.

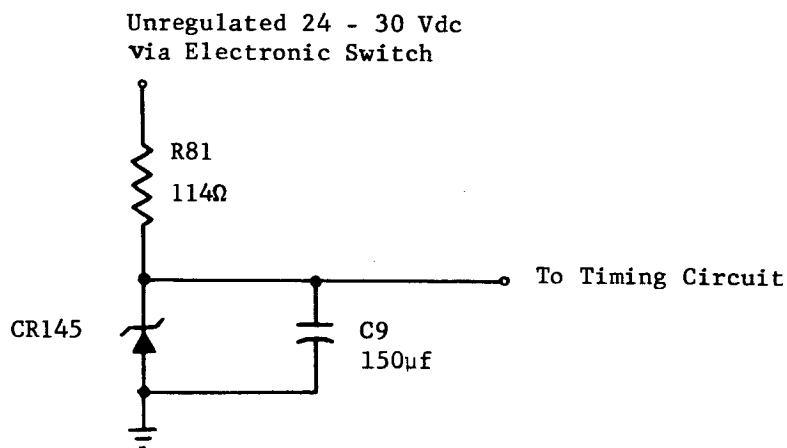


Figure 32. Regulated Six-volt dc Supply (Modified Version)

Remarks: The modified six-volt supply is simpler in design than the original version. It also provides for an increase in load over the original version and eliminates any unnecessary power dissipation when operating at its load capacity of 145 ma. Its nominal efficiency ranges from 9.3% for an output current of 65 ma to a maximum of 23.4% at 145 ma. The output voltage will be within 6.5 and 7.2 vdc for all expected conditions, and the supply will function as a low impedance zener voltage source for the minimum input voltage, i.e., 24 vdc. The zener diode, operating in the breakdown mode, will attenuate any ripple on the input voltage; and, with capacitor C9 on the output, the output voltage ripple is expected to be negligible. From the stress analysis of Section 3.3.1.3 all components operate well within their rated capabilities.

The failure mode and effects analysis in Section 3.3.1.2 identifies a potential improvement in the simpler, modified design. The modified version represents a slight loss of advantage on the basis of simple failure logic over the original version by separating the redundant supplies in this manner. However, it is shown in Section 3.3.1.1 that within the limits of precision of failure rate data, there is no significant difference in the overall inverter success probability.

The modified electronic switch has not been breadboarded and no experimental observations have been made.

3.3.4.2 Electronic Switches

3.3.4.2.1 Original Version (Elements 22 and 23)

Schematic: Element 22 is shown in Figure 33. Element 23 is identical.

Function: Close the 6 volt supply to the timing generator or open the 6 volt supply from the timing generator if the alternate channel is active.

Inputs: (1) 6 vdc from the six-volt supply.
(2) zero or 6 vdc to the alternate channel electronic switch (element 23).
(3) two complementary, positive going 400 cps square waves from the alternate channel Pulse Sequence Generator (element 31).

Load: Nominally 65 ma total at 6 volts to the timing generator elements and the alternate channel electronic switch.

Attributes: (1) output voltage.
(2) output voltage ripple.

Remarks: The original design of the electronic switch is adequate. As an open switch, the base-emitter junction of Q22 is reverse biased by approximately 3 volts

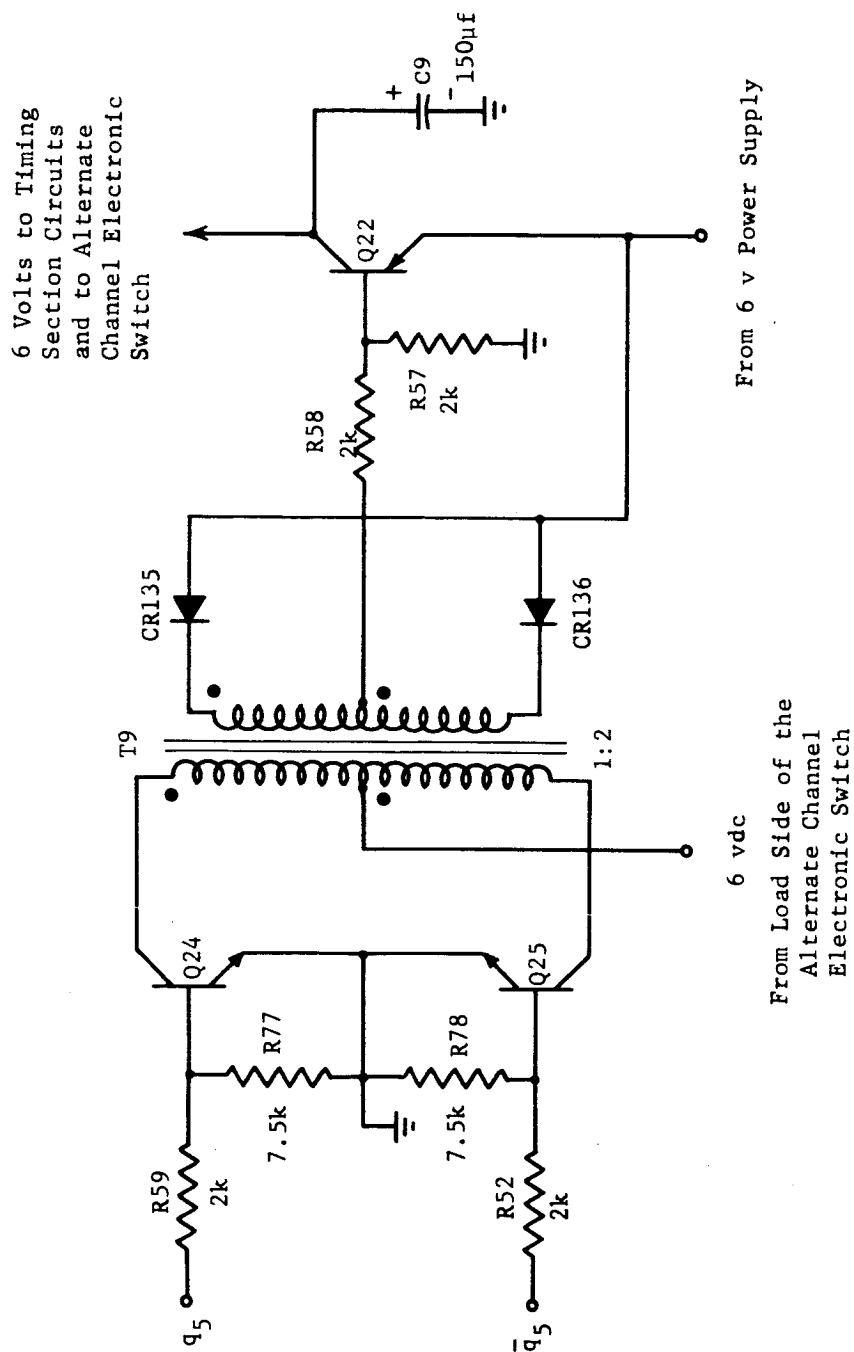


Figure 33. Electronic Switch (Original Version)

and the collector (switch) current is negligible. In the absence of the complimentary hold-open signals from the alternate timing generator, Q22 will become forward biased and approximate a closed switch in the six-volt bus. The voltage output of the electronic switch is reduced by the $V_{CE(sat)}$ drop of Q22. The output voltage will remain between 5.8 and 7.4 vdc for all expected input conditions, and the output voltage ripple is filtered to a negligible level by C9. The stress analysis of Section 3.3.1.3 shows that all components are applied well within their rated capabilities.

Continuing with the data recorded for the original 6 volt supply, the closed electronic switch has been observed to supply 51.5 ma at 6.42 volts to the associated timing circuit from an input of 63.8 ma at 7.25 volts from the 6 volt supply. The difference between the input and output currents is the current supplied to forward bias Q22 and to operate the alternate channel switch.

3.3.4.2.2 Modified Version (Elements 22M and 23M)

Schematic: Element 22M is shown in Figure 34. Element 23M is identical.

Function: Close the primary voltage source to the six-volt supply, or open the primary voltage source to the six-volt supply in the event that the alternate timing generator is active.

Inputs: (1) 28 vdc from the primary voltage source.
(2) zero or 28 vdc from the alternate channel electronic switch.
(3) two complimentary, positive going 400 cps square waves from the alternate channel pulse sequence generator (element 31).

Load: 28 volts at 220 ma total to the six-volt supply and the alternate channel electronic switch.

Attributes: Output voltage.

Remarks: The configuration of the modified electronic switch is identical to that of the original version except that the Q22 collector-emitter capacitor (C9 in Figure 33) has been removed and capacitor C16 has been added across the base-emitter terminals of Q22 in the modified switch (Figure 34). Since the modified switch controls the 28 vdc and supplies it to the six-volt supply rather than controlling the 6 vdc to the timing generator elements, the output voltage ripple is of much less concern and ripple introduced by the periodic demand of the alternate channel electronic switch will be acceptable. C16 will isolate the switch from any effects of ripple introduced by the hold-open circuit.

A complete review of the modified switch is not possible because the design of T9 is unknown. However, some conservative assumptions have been made concerning

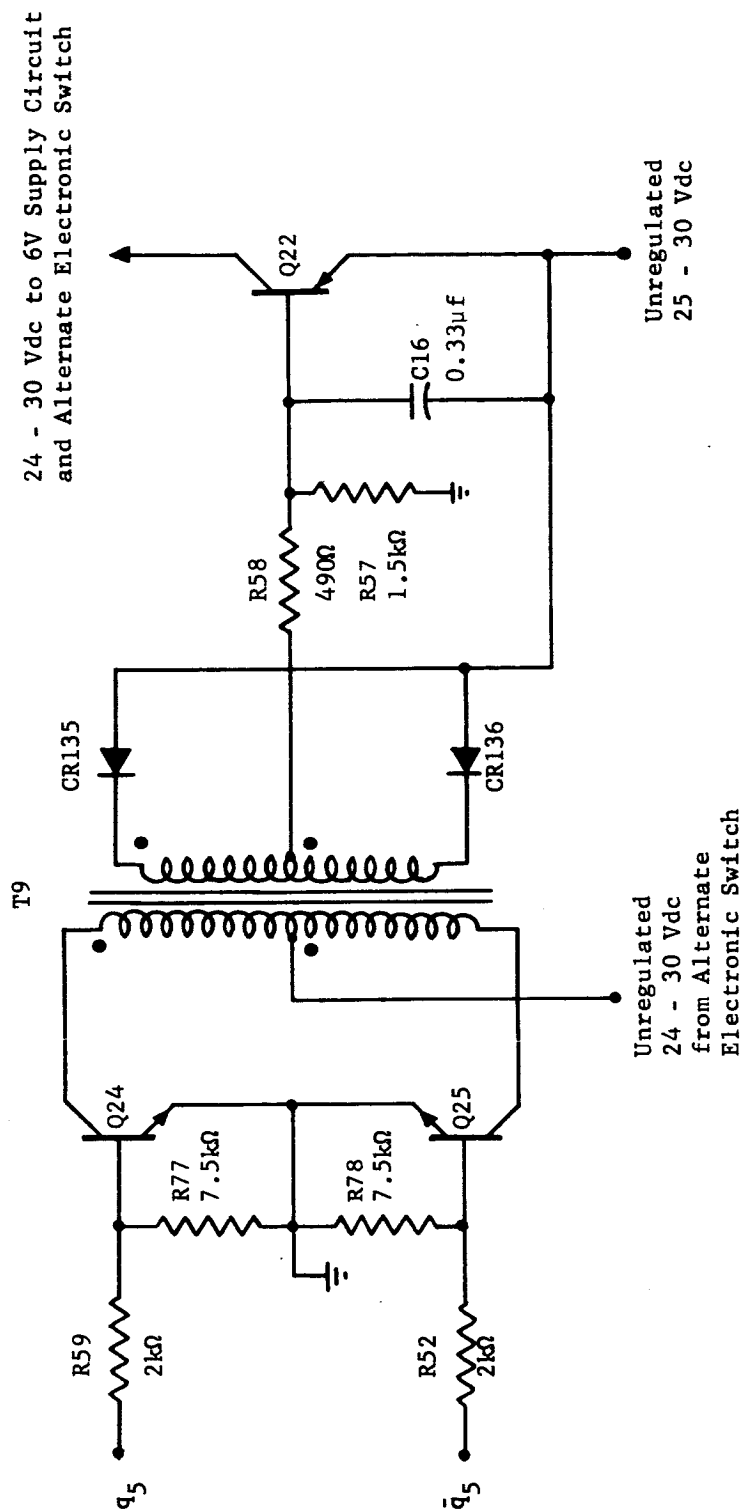


Figure 34. Electronic Switch (Modified Version)

the design requirement and an analysis completed. Since this analysis has not been included elsewhere, some of the details are included herein.

When operating as a closed switch, the hold-open circuit of the modified electronic switch is inactive, and the minimum base drive to Q22 (2N3204) is estimated to be

$$I_{B(\min)} = \frac{(25 - 1)V}{1576\Omega} = 15.25 \text{ ma.}$$

Assuming a minimum worst-case h_{FE} of 20, I_B will saturate the switch for a maximum collector current of

$$I_{C(\max)} = (20) (15.25) \text{ ma} = 205 \text{ ma.}$$

The maximum I_C , i.e., switch current, will be less than 200 ma.

In open-switch mode of operation, a reverse bias of 3 volts across the base-emitter junction of Q22 will give an open circuit. Therefore, the secondary center-tap voltage must be

$$V_{CT} = 33V \times \frac{1940\Omega}{1425\Omega} = 45 \text{ volts,}$$

and the secondary induced voltage must be

$$V_S = (45V - 30V + 1V) = 16 \text{ volts.}$$

Therefore, the required transformer turns ratio can be determined as

$$\frac{N_S}{N_P} = \frac{V_S}{V_P} = \frac{16}{25} = 0.64.$$

The maximum T9 secondary current will be approximately

$$I_{\text{sec}} \approx \frac{30V + 16V - 1V}{465\Omega + 1425\Omega} = \frac{45}{1.89} \text{ ma} = 23.8 \text{ ma,}$$

and the maximum primary current will be

$$I_{\text{pri}} \approx 0.64 \times 23.8 \text{ ma} = 15.2 \text{ ma.}$$

The T9 primary current is the required collector current for Q15 and Q16 (S2N2034A's). Assuming a minimum worst-case h_{FE} of 20, the required base current will be

$$I_{B(Q15, 16)} = \frac{15.2 \text{ ma}}{20} = 0.76 \text{ ma.}$$

This requirement is compatible with the driving flip flop (SN511A) capabilities.

The component stress analysis in Appendix E shows that all components are applied well within their capabilities for the conditions assumed in the preceeding analysis.

Since the modified electronic switch has not been breadboarded, no experimental observations have been made of the circuit.

3.2.4.3 Primary Oscillators (Elements 24 and 25)

Schematic: Figure 35.

Function: Provide a 76.8 kc signal to the frequency countdown circuit suitable for switching the first stage flip flop.

Input: 6 vdc from the six-volt supply.

Load: First stage flip flop of the frequency countdown circuit.

Attributes: (1) Output frequency stability
(2) Output signal amplitude
(3) Output signal fall time

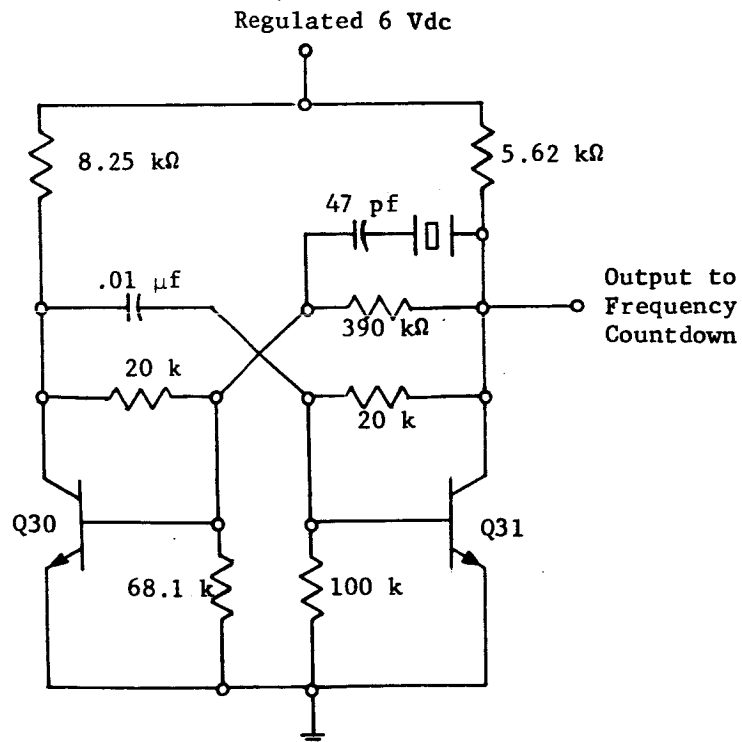


Figure 35. 76.8 kc Primary Oscillator

Remarks: Since the inverter output frequency is completely determined by the primary oscillator, the output frequency of the oscillator is its most important attribute. The oscillator frequency is, in turn, controlled solely by the crystal which is selected to meet the required specifications. Since it is anticipated that the primary frequency source will be redesigned, little attention was given to the primary oscillator except to note its attributes and that no component in the oscillator is stressed appreciably with respect to its rated capacity.

In Section 3.3.3.2, it is noted that when the static inverter is first turned on or when it is caused to switch from one redundant timing generator circuit to the other, a distinct shift in output frequency occurs. The inverter frequency is initially greater than 400 cps, e.g., 480 cps, 525 cps and 600 cps; and their durations have been for several cycles, e.g., 10. The change from the initial output frequency back to the 400 cps is a step function.

The source of the output frequency shift has been traced to the primary oscillator where the change occurs more linearly over many cycles. Since the ratio of the oscillator frequency to the 400 cps output frequency is 192, a shift in the oscillator frequency occurring over many cycles would appear as a step change in the 400 cps output.

Except for the experimental observations noted above, no further study has been made of the frequency shift. The shift is assumed to be a characteristic of the crystals in the oscillators. The complete transient is difficult to observe at the oscillator, and a thorough study is not justified since the primary oscillator will be replaced. Although the criticality of the observed frequency transient is not known, numerous difficulties could result from an initial "low" frequency that permitted the square-loop transformers to saturate.

3.3.4.4 Frequency Countdown Circuit (Elements 26 and 27)

Schematic: Figure 36.

Function: Reduce the crystal controlled 76.8 kc primary oscillator signal to a 4.8 kc signal.

Inputs: (1) 6 vdc from the six-volt supply.
(2) 76.8 kc, 1.5 volt square wave from the primary oscillator.

Load: (1) Two complementary, positive going 4.8 kc square waves to the magnetic amplifier driver circuit.
(2) From a parallel output stage, a 4.8 kc positive going square wave to the clock pulse amplifier.

Attributes: Output amplitude.

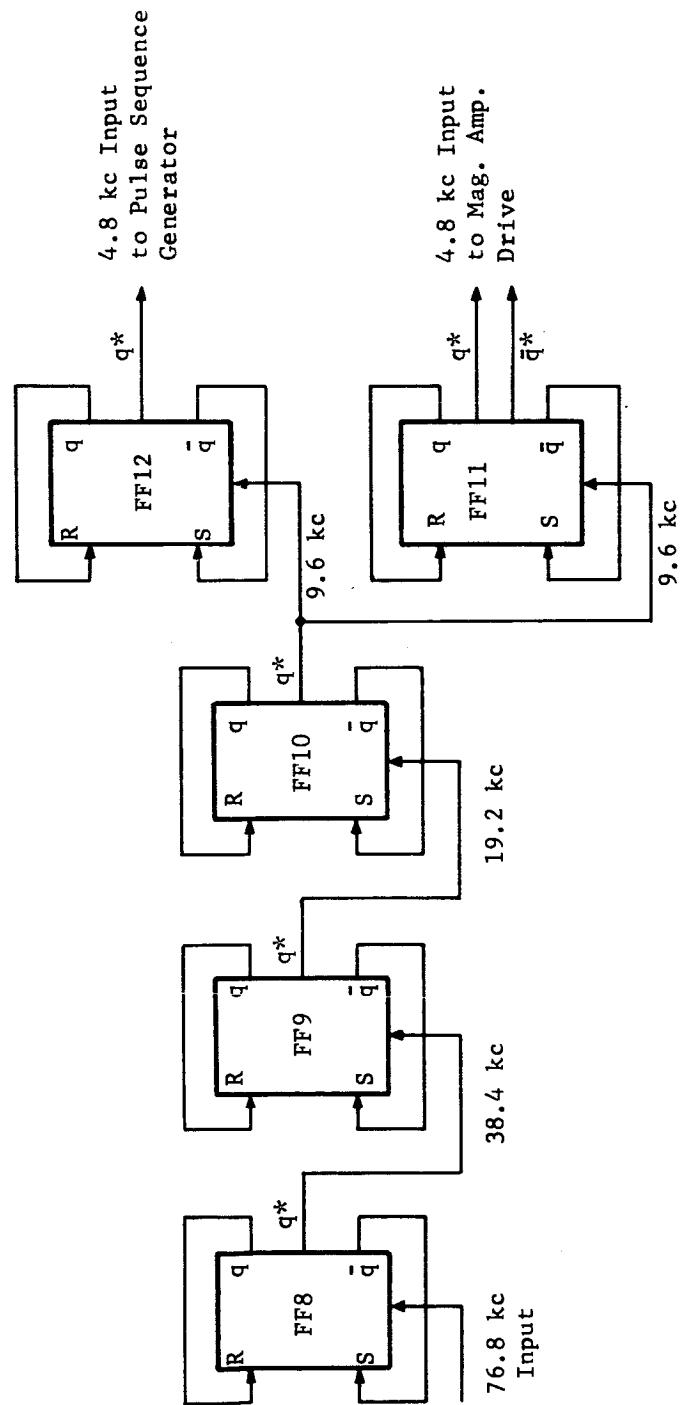


Figure 36. Frequency Countdown Circuit

Remarks: The preliminary design review [Ref. 2] concluded that the design of the frequency countdown circuit conformed to a design configuration recommended by the manufacturer of the SN511A networks and to the application rules stated by the manufacturer. The remaining area of interest is the interface between the frequency countdown and other elements of the inverter. It was concluded that the input from the primary oscillator was satisfactory and the clock pulse amplifier was an acceptable load. The interface between the frequency countdown and the magnetic amplifier driver circuit has been examined in detail [Ref. 3], and it is concluded that the design is adequate for both the original configuration and the modification recommended therein.

Some further discussion of the SN511A networks is appropriate at this point. From the measured characteristics of these flip flops, it was observed that all units had lower output impedances than claimed by the manufacturer [Ref. 3]. The switching times were not measured for individual units because switching times of these circuits are more than adequate for the relatively low switching frequencies in this application.

In Section 3.3.4.6 some observed difficulties with the SN511A networks in the pulse sequence generator application are described. Similar difficulties were not observed for the frequency countdown circuit application; in fact, malfunctioned units from the pulse sequence generator were observed to operate normally when placed in the frequency countdown circuit.

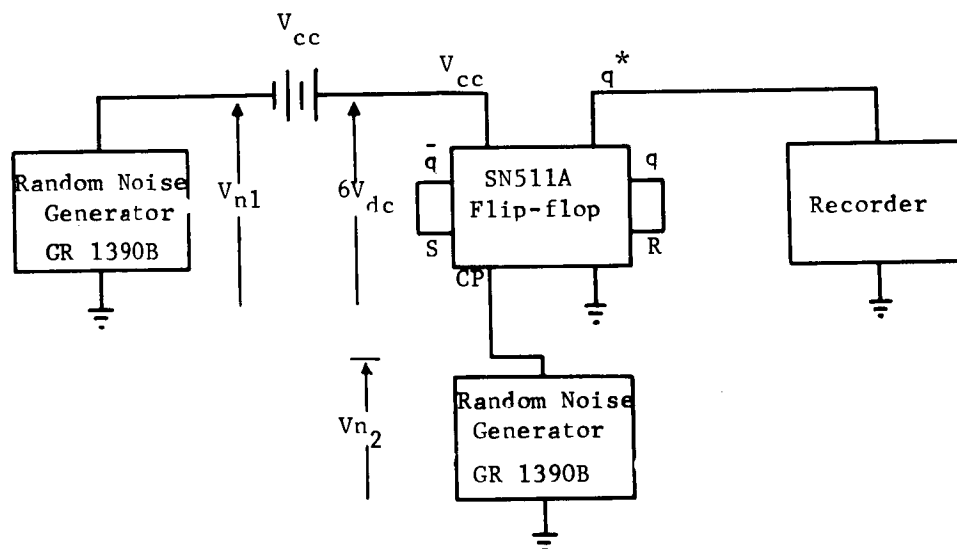


Figure 37. SN511A Noise Experiment

The block diagram of Figure 37 illustrates a simple experiment performed to gain some familiarity of SN511A flip flop sensitivity to noise. With $V_{n1} = V_{n2} = 100$ mv rms, the flip flops under test changed states frequently. With $V_{n1} = V_{n2} = 60$ mv rms, the flip flop under test averaged changing states seven times in a 24 hour period, and two times in a 24 hour period for $V_{n1} = V_{n2} = 40$ mv rms. The experiment described was not extensive enough to justify any conclusions, and the results are included here as a matter of interest.

Flip flop failures that occurred during the course of this project are reported in Appendix G.

3.3.4.5 Clock-pulse Amplifier (Elements 28 and 29)

Schematic: Figure 38.

Function: Reduce the amplitude of the 4.8 kc output from the frequency count-down circuit for driving the pulse sequence generator.

Input: (1) 4.8 kc square wave from the frequency countdown circuit.
(2) 6 vdc from the six-volt supply.

Load: Pulse Sequence Generator, i.e., six R-S flip flop clock pulse terminals.

Attributes: (1) Output amplitude.
(2) Output pulse fall time.

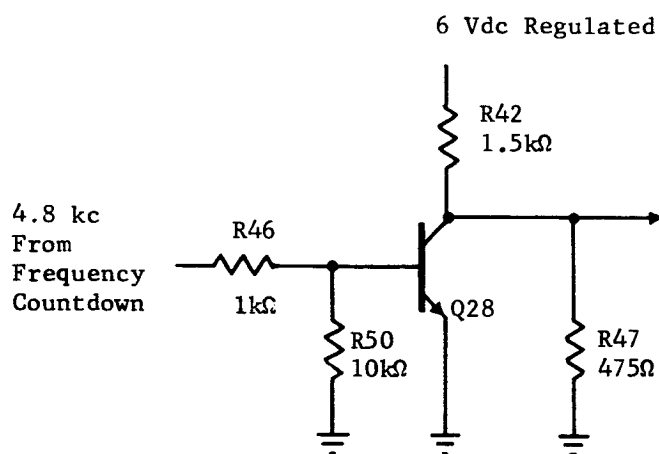


Figure 38. Clockpulse Amplifier

Remarks: It was previously concluded [Ref. 2] that the design of the clock pulse amplifier (CPA) was adequate in all respects. The high-level output pulse voltage is between 1.47 and 1.76 volts (adequate for the clock pulse input to the pulse sequence generator) for all expected conditions, and all components are applied within their rated capabilities.

It was previously suggested [Ref. 2] that the CPA might possibly be eliminated since it was concluded from the SN511A manufacturer's data sheet that the SN511A output from the frequency countdown circuit was adequate to drive the clock pulse input to the pulse sequence generator. Experimentally, the CPA was removed from one of the timing generator circuits and the inverter was caused to operate with that timing generator active. The operation was intermittent as required by the test program. The inverter operated satisfactorily at the expected temperature extremes without switching to the normal timing generator. As described in detail in Section 3.3.4.6, frequent difficulties with the pulse sequence generator were observed starting after several months of operation in this manner.

After several failures of the type described, the CPA was replaced and the difficulties terminated. It was then concluded that the CPA is essential to the reliable operation of the pulse sequence generator. After replacing the CPA, however, additional failures of the pulse sequence generator have occurred. Since the difficulties described for the pulse sequence generator have not been resolved, it is recommended that use of the CPA be continued.

The CPA was also used as a test circuit to investigate the NET-1 computer program for circuit analysis. The circuit was loaded by a circuit simulating the SN511A flip flop and both transient and steady-state analyses performed. Except for the evaluation of the computer analysis technique itself, the only additional information of utility from this effort was further verification that switching transients for the low frequency application involved are of no concern.

3.3.4.6 Pulse Sequence Generator (Elements 30 and 31)

Schematic: Figure 39.

Function: To convert the 4.8 kc clock pulse from the clock pulse amplifier to a train of six positive-going 400 cps square waves, and a logical complement of each, that are phase displaced by 30 electrical degrees.

Input: (1) 6 vdc from the regulated six-volt supply.
(2) 4.8 kc positive going square wave from the clock pulse amplifier.

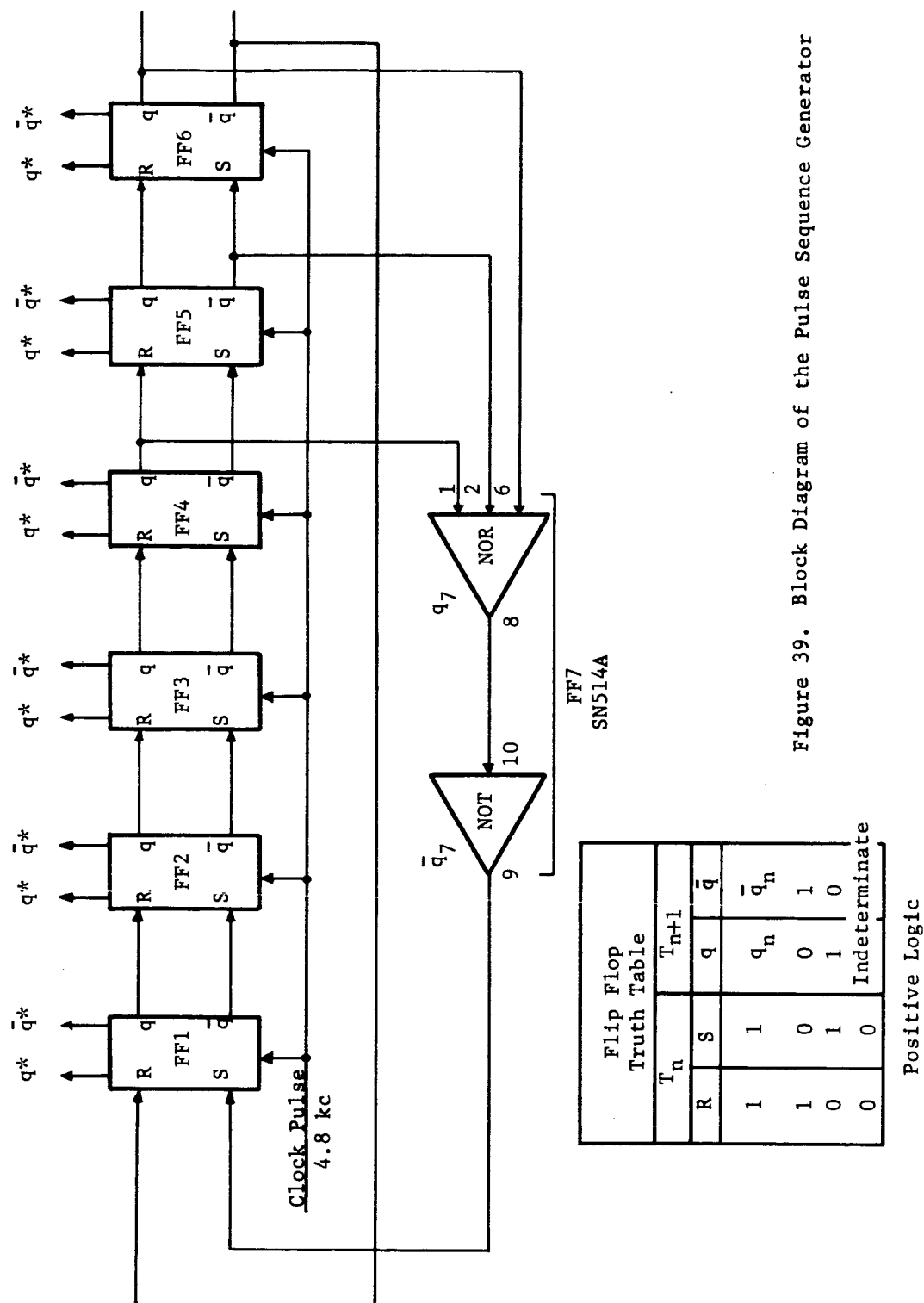


Figure 39. Block Diagram of the Pulse Sequence Generator

Load: Each flip flop in the pulse sequence generator drives a timing pulse amplifier via the coupling circuits (elements 34 - 45). In addition one flip flop in each of the timing generators (elements 38 and 44) drives the alternate generator electronic switch as a parallel load.

Attributes: (1) Output voltage.
(2) Output current.

Remarks: The application of the six SN511A and single SN514 networks in the pulse sequence generator (PSG) conforms to the application rules recommended by the manufacturer, and the PSG design configuration is nearly identical to a Johnson counter arrangement also recommended [Ref. 10]. In a design reliability study of the PSG load circuits [Ref. 3], the SN511A networks were considered adequate as driving sources for the timing pulse amplifiers. From all application considerations the design of the PSG is considered sound; however, there have been certain difficulties observed during breadboard circuit operation which preclude firm conclusions with regard to design adequacy without further detailed investigation. These difficulties are described in more detail below.

As described in Section 3.3.4.5, the clock pulse amplifier (CPA) was removed from one of the timing generator circuits in the inverter breadboard to experimentally assess the feasibility of its elimination. In addition to pulse shaping, the CPA normally provides a high-level clock pulse voltage between 1.47 and 1.76 volts. According to the SN511A network manufacturer's data sheet, the input clock pulse amplitude can exceed the V_{cc} voltage, 6 vdc minimum in this case. The required threshold amplitude is less than 1 volt, thus the normal CPA output is adequate as a clock pulse input to the PSG. With the CPA removed and the clock pulse input provided directly from an SN511A emitter follower output in the frequency countdown circuit, the high-level pulse amplitude is typically 3.6 volts and the pulse shape is considered acceptable for a clock pulse.

With the CPA removed from one of the redundant timing generator circuits, breadboard circuit operation was always initiated so that that circuit was active. Operation was intermittent as required by the test program. The breadboard continued to operate successfully at room temperature and during special tests under low and high ambient temperature extremes without switching to the timing generator which still contained a CPA.

After a period of several months of intermittent operation, malfunctions began to occur which were usually manifested by failures in the timing pulse amplifiers. Further investigations revealed these failures to result from lack of symmetry in duty cycle in the complementary driving signals from the PSG flip flop outputs.

By trial and error the individual flip flop causing the discrepancy could be located, and when replaced with new units, operation would resume normally. The discrepant flip flop units appeared to function normally in a test circuit and also operated successfully when placed in the frequency countdown circuit.

After several failures of this type, the CPA was replaced in the circuit, returning the input clockpulse waveform and amplitude to normal. The PSG operation resumed normally, even with the flip flop units which had previously malfunctioned. At this point, it was concluded that the amplitude of the input clockpulse is critical, and should be considerably less than the V_{cc} voltage. A later letter communication from the SN511A network manufacturer confirmed only that the input clockpulse input should be less than the V_{cc} voltage. Verbal communication with some users revealed an undocumented application rule of about $V_{cc}/3$ as a good clockpulse amplitude. It was thus concluded that the CPA was critical to reliable operation of the inverter and should be employed. Due to the success achieved with the frequency countdown circuit this same restriction does not appear to apply to the SN511A networks in that application.

While continuing breadboard operation with the CPA included, further discrepancies of the type described above have been observed. This has occurred with the PSG circuit in both timing generator circuits, but because flip flop units had been freely interchanged without keeping track of individual units it is not possible to identify whether these additional discrepancies were caused by the same units that had previously malfunctioned. The problems associated with this observed phenomena have thus not been resolved and it cannot be firmly concluded that the trouble resulted solely from the input clockpulse amplitude. The flip flops have obviously degraded with time and operation; however, no quantitative measure of degradation can be stated.

The problem described above introduces much uncertainty in the performance capability of the PSG and will require more study for resolution. The most logical approach is a test program to measure the effect of extended operation under different conditions. A considerable amount of design information and assurance could result from constructing several circuits with the PSG configuration and operating these under controlled conditions of clock pulse amplitude, V_{cc} voltage, flip flop load and ambient temperature with the experiment designed to include several levels of each. The pulse duty cycle of either flip flop output should be monitored to observe for malfunctions. Use of the PSG configuration (or a similar one providing closed loop operation of the flip flops) is emphasized because it is possible that the recycling loop arrangement may be the main stimulus giving rise to the observed anomaly. This suspicion is generated to some extent by the fact that malfunctioning

units operated successfully as flip flops in open loop in a test circuit and in the frequency countdown circuit. Further checks of this effect could be made by conducting a parallel experiment with the tests described above to test some units in open loop.

The existing uncertainty in the PSG performance provides adequate justification for employing redundancy in the timing section even though the comparison of predicted mission success probabilities with and without redundancy computed in Section 3.3.1.1 shows only slight improvement.

3.3.4.7 Coupling Circuits

3.3.4.7.1 Original Version (Elements 32 - 45)

Schematic: Figures 40 and 41.

Function: Couple the active timing generator to the timing pulse amplifiers (TPA's) and the magnetic amplifier driver circuit, and to isolate the inactive timing generator from the active timing generator.

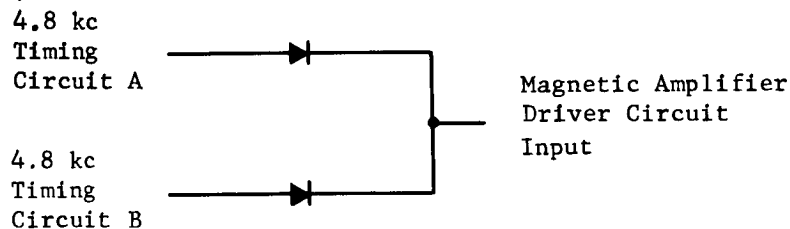


Figure 40. Coupling Circuit (Original Version) Between the Frequency Countdown Circuits and the Magnetic Amplifier Driver Circuit (Elements 32 and 33)

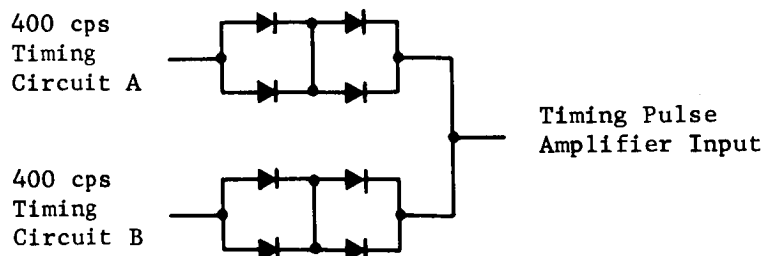


Figure 41. Coupling Circuit (Original Version) Between the PSG Outputs and the Timing Pulse Amplifiers (Elements 34-45)

Input: (1) Positive-going 4.8 kc square waves to elements 32 and 33 from the frequency countdown circuit.

(2) 400 cps square waves to elements 34 - 45 from the PSG.

Load: Less than 10 ma to both the TPA's and the magnetic amplifier driver circuit.

Attributes: Forward voltage drop.

Remarks: The coupling circuits form diode OR gates to connect the active timing generator to the timing pulse amplifiers (Figure 43) and the magnetic amplifier drive circuit (Figure 53) while isolating the inactive timing generator. The output voltage levels from the inactive timing generator are nominally zero, and the output voltage levels from the active timing generator are positive. Consequently, the coupling circuit diodes between the inactive timing generator and the coupling circuit loads are reverse biased.

It was concluded that the base drive current to the TPA's for worst-case conditions was inadequate [Ref. 2]. Subsequent analyses with improved component data confirmed this conclusion and a modification of the coupling circuit and the TPA input circuit was suggested to provide for an increased minimum value of base current to the TPA transistors [Ref. 3]. Since the proposed modification also increased the reliability of the circuit, it was also proposed as a modification for the magnetic amplifier drive circuit and its associated coupling circuits. The modified coupling circuits are discussed in the following section.

3.3.4.7.2 Modified Version (Elements 32M - 45M)

Schematic: Figure 42.

Function: Same as original version.

Inputs: Same as original version.

Load: Same as original version.

Attributes: Resistance.

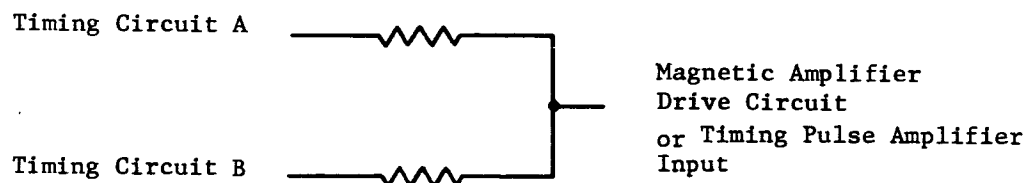


Figure 42. Coupling Circuit--Modified Version (Elements 32M-45M)

Remarks: The modified coupling circuits resistively couple the timing generator circuits to the TPA's and the magnetic amplifier drive circuit. In both cases, the diode OR gates are removed and the two timing generators are coupled to the modified TPA's and the modified magnetic amplifier drive circuit through paralleled resistors. The modified configurations are discussed in detail in Section 3.3.4.8.2 and in Section 3.3.4.14.2 and it is concluded that the modifications provide for adequate transistor base drive to the loading elements, adequate isolation between the two timing generators, and increased circuit life [Ref 3].

3.3.4.8 Timing Pulse Amplifier

3.3.4.8.1 Original Version (Elements 46 - 51)

Schematic: Figure 43.

Function: Amplify the complementary 400 cps positive-going square wave outputs of the PSG to provide adequate drive for the power converter stages.

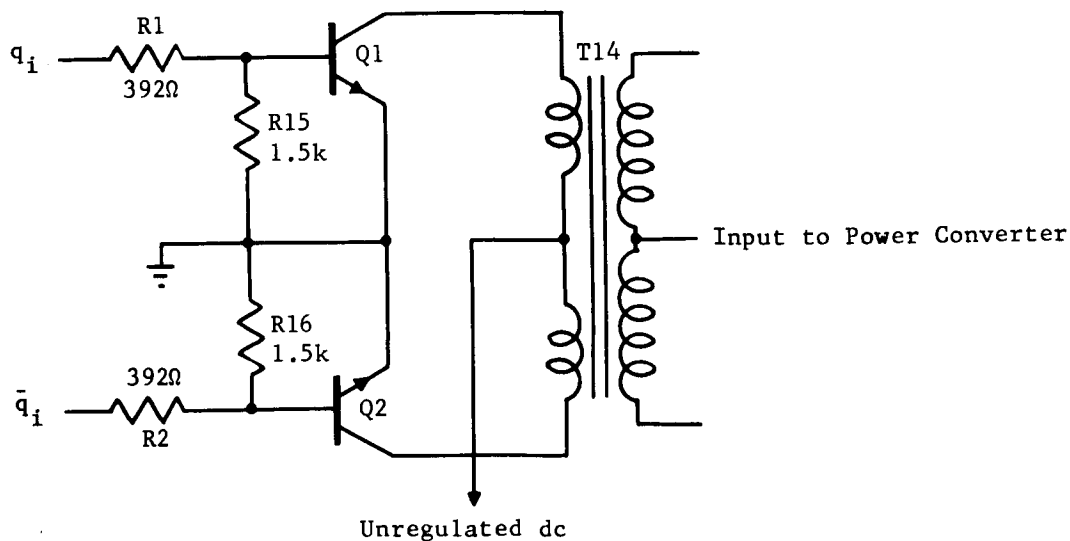


Figure 43. Timing Pulse Amplifier (Original Version)

Inputs: (1) Complementary 400 cps positive-going square waves from the PSG.
(2) Unregulated dc inverter input; nominally 28 vdc.
Load: Base-emitter circuits of the power converter stages.
Attributes: (1) Output voltage amplitude.
(2) Output current.

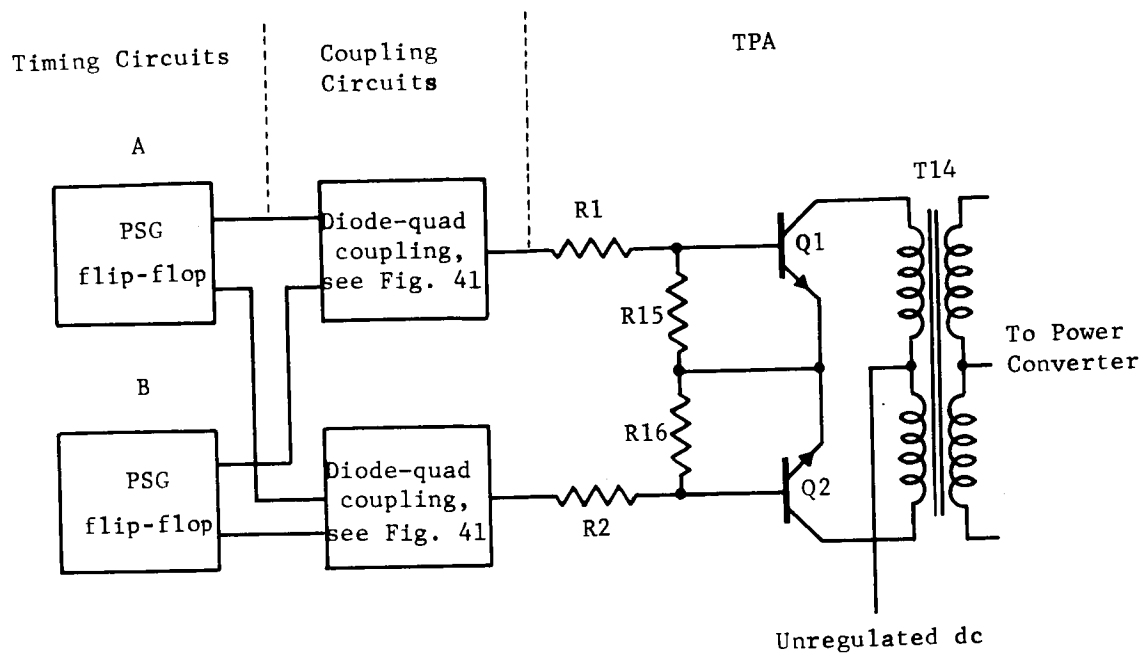
Remarks: An analysis of the timing pulse amplifier (TPA) circuit concluded that the base drive to the TPA transistors was inadequate [Ref 2]. Subsequent analyses with improved component data confirmed the inadequacy of the worst-case base drive to the TPA transistors, and the base drive problem was examined in detail [Ref. 3]. It was suggested that the minimum base drive current be increased by modifying the coupling circuits between the PSG's and the TPA's, and modifying the TPA input circuit. The suggested modification was examined in detail [Ref. 3] and is described briefly in the following section. In all other respects, the design of the TPA is adequate and all components are applied within their rated capabilities.

3.3.4.8.2 Modified Version (Elements 46M - 51M)

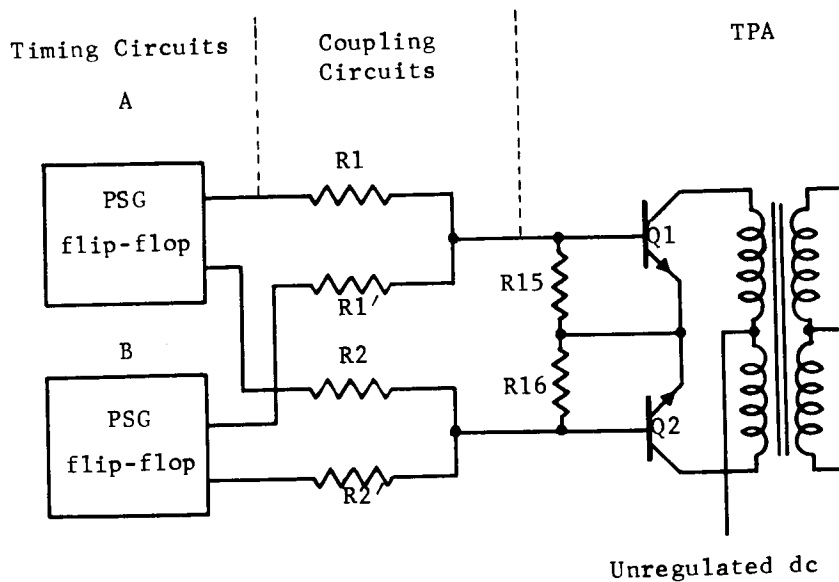
Schematic: Figure 44.
Function: Same as original version.
Inputs: Same as original version.
Loads: Same as original version.
Attributes: Same as original version.

Remarks: Figure 44 illustrates the TPA modification for element 46M. In this version, the original diode coupling circuits are replaced by resistive networks that include the base input resistors of the original TPA's. The PSG flip flops from one timing generator drive the TPA transistors through the original base circuit resistors, e.g., R1 and R2 in Figure 44, and the PSG flip flops from the second timing generator couple to the TPA transistors through resistors added in parallel with the original TPA base circuit resistors. In the original version of the TPA's, R1 - R12 are 392 Ω resistors. In the modified versions, these resistors are in the coupling circuits and their values are changed. R1 - R8, R11 - R12, R1' - R8' and R11' - R12' are 582 Ω resistors; and R9, R10, R9' and R10' are 476 Ω resistors. The latter four resistors are associated with the PSG flip flops that also drive the electronic switches as parallel loads.

It has been demonstrated that the modified configuration provides adequate isolation between the active and the inactive timing circuits, adequate base drive for the TPA transistors under worst-case conditions, and increased reliability.



Original Version



Modified Version

Figure 44. Illustration of the TPA and Coupling Circuit Modification

3.3.4.9 Power Converters (Elements 52 - 57)

Schematic: Figure 45.

Function: Convert the controlled dc voltage to the three-phase, 400 cps output voltage.

Inputs: (1) Complementary, 400 cps square waves from the timing pulse amplifiers.
(2) Controlled dc voltage from the voltage regulator circuit.

Load: Inverter output load via the output circuit.

Attributes: Voltage amplitude.

Remarks: Although an analysis of the power converters was previously reported [Ref. 2], some of the conclusions of that analysis were based upon typical or measured component characteristics which have subsequently been updated. Since some of the conclusions of the original analysis have also been modified, the analysis is repeated here.

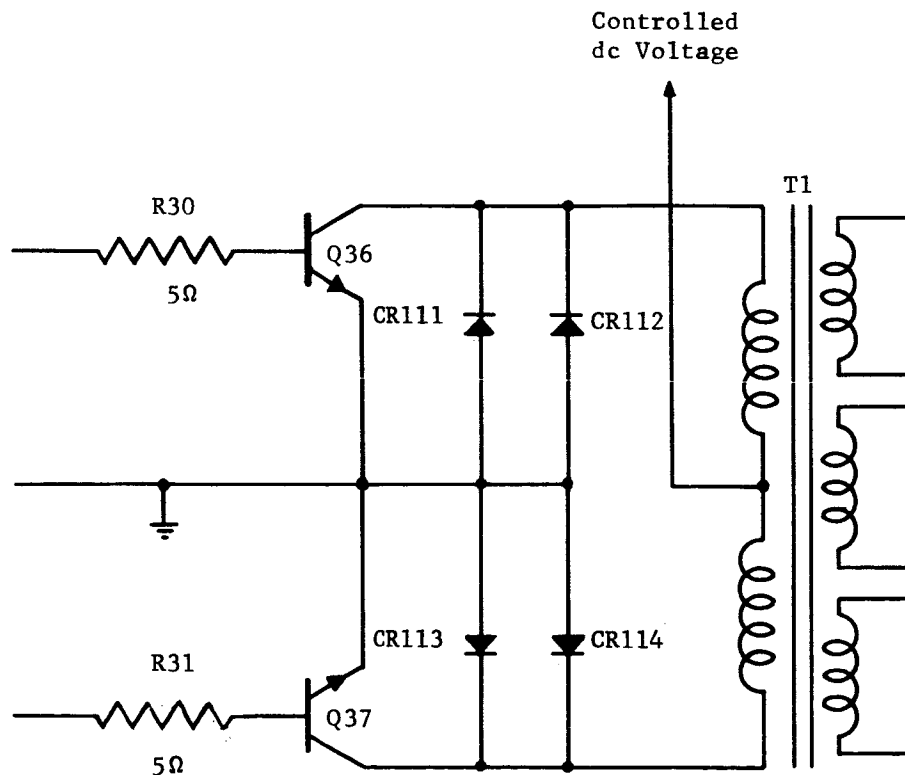


Figure 45. Power Converter

With a 250 va load and assuming an efficiency of 80% for the combined output circuits and power converters, each power converter stage must supply a load of

$$P_L = \frac{250 \text{ va}}{0.80 \times 6} = 52 \text{ va.}$$

The dc voltage varies with load, and is approximately 20.8 volts at rated load (resistive) and approximately 18.2 volts at no load. Assuming a maximum $V_{CE(sat)}$ of 1.0 volt for Q36 and Q37, the average collector current per transistor is estimated as

$$I_{C(avg)} = \frac{52 \text{ va}}{(20.8 - 1.0)\text{v} \times 2} = 1.31 \text{ amperes.}$$

This neglects the current through the reactive diodes which results from the phase difference between the transistor voltage and current. The three-phase inverter output voltage is sinusoidal, and the output current to a linear load will also be sinusoidal. Consequently, the currents in the transformer windings will also be sinusoidal. The peak primary current which is also the peak collector current in Q36 will be

$$I_{C(peak)} = 2.62 \text{ a} \times \frac{1}{.637} = 4.12 \text{ amperes}$$

where 2.62 a is the half cycle average collector current and 1/.637 is the ratio of the peak value of a sinusoid to its half cycle average.

The minimum base current to the power converter transistors is estimated to be

$$I_{B(min)} = \frac{(25 - .3)\text{v} \frac{54}{340} - 1.1 \text{ v}}{[20(\frac{54}{340})^2 + .75 + 5.5] \Omega} = 4.5 \text{ ma,}$$

where

- 25 v = minimum input voltage,
- 0.3 v = $V_{CE(sat)}$ for Q1 and Q2,
- 54/340 = ratio of secondary to primary turns on T14,
- 1.1 v = maximum V_{BE} for Q36 and Q37,
- 20 Ω = T14 primary winding resistance,
- 0.75 Ω = T14 secondary winding resistance, and
- 5.5 Ω = maximum value of R30.

Consequently, a dc gain, h_{FE} , value of ten (10) will saturate these transistors for worst-case conditions. Originally, 2N1016D transistors were specified and are in the breadboard model. The most recent revision specifies a 2N3432. The rated h_{FE} for both transistors has a minimum value of 10 at 5 amperes of collector current and at 25°C, and increases with both decreasing temperature and decreasing collector current in that region. From available data, it is concluded that h_{FE} will be greater than 10 at the lower, worst-case collector current and 100°C and, consequently, adequate for all conditions of interest. It is recommended, however, that the transistors used for this application be screened to ascertain that the gain is adequate.

The 2N1016D and the 2N3432 are similarly rated for all electrical characteristics of interest and are adequate for this application.

It was noted in the component stress analysis of Section 3.3.1.3 that the reactive diodes, i.e., CR111 - CR134, were required to conduct more than their rated currents. For a zero power factor load, for example, the reactive diodes are required to conduct for 1/2 of each cycle as illustrated in Figure 46. Consequently, for these conditions each of the reactive diodes must conduct an average current of

$$\begin{aligned} I_{d(\text{avg})} &= \frac{1}{4} I_{C(\text{avg})} \\ &= 0.325 \text{ amperes,} \end{aligned}$$

and a peak current of

$$\begin{aligned} I_{d(\text{peak})} &= \frac{1}{2} I_{C(\text{peak})} \\ &= 2.06 \text{ amperes.} \end{aligned}$$

Consequently, the reactive diodes are inadequate for the worst-case peak recurrent currents required of them. In the event that one diode fails by opening, the requirements are doubled for the parallel unit and it too will probably fail in a short time. It is recommended that a suitably rated single diode be used as a replacement for each of the parallel pair of reactive diodes.

It was previously suggested the power dissipation in the power converters could be reduced without influencing performance or reliability by reducing the secondary turns on T14 - T19 in the output of the timing pulse amplifiers and also reducing the resistance value of R30 - R41 [Ref. 2]. Such a modification would decrease internal power dissipation by, for example, approximately 3 watts out of 190 watts.

The component stress analysis of Section 3.3.1.3 illustrates that the design of the power converters is satisfactory in all other respects.

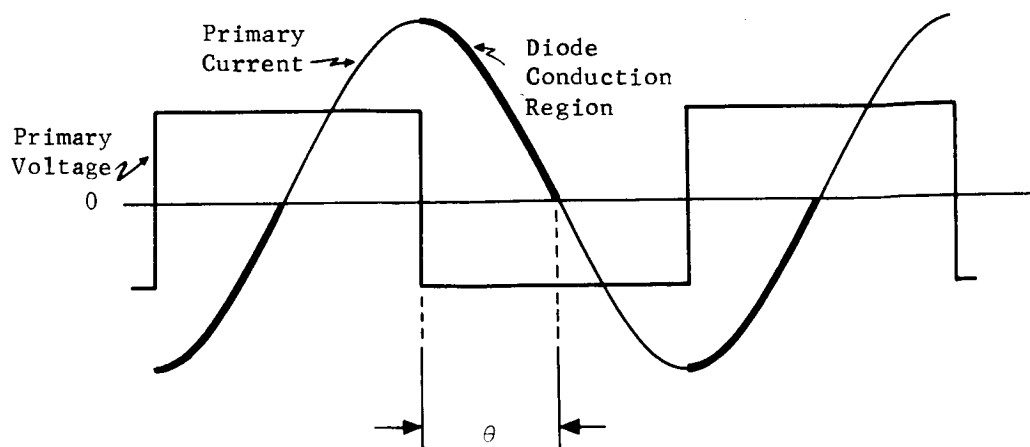
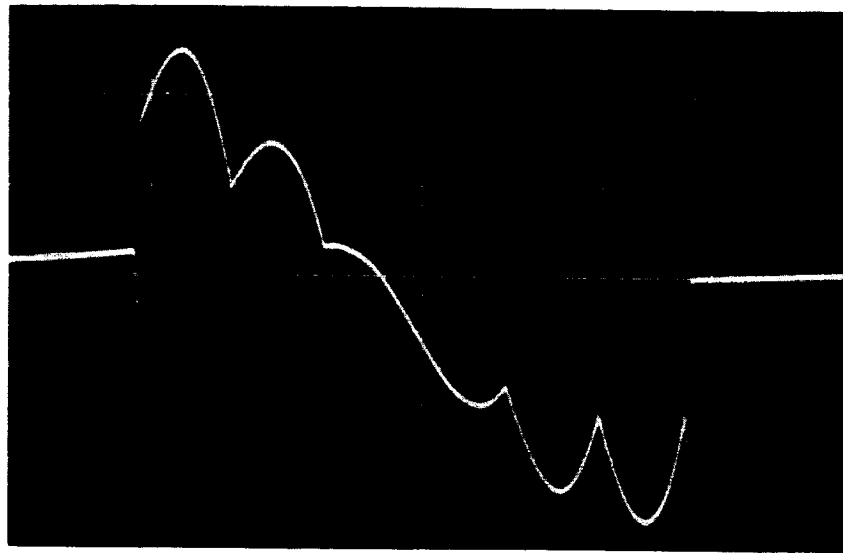


Figure 46. V-I Relationship in the Output Transformer Primary Winding Illustrating Reactive Diode Conduction.

Figures 47 and 48 illustrate the performance of the power converters for a typical application. Figure 47 shows the total current in one primary winding of T1 and the total reactive diode current, i.e., current in CR111 and CR112 for a 125 va resistive load. The average total diode current in Figure 47 is estimated to be 28 ma, and the peak current is 700 ma. Figure 48 shows the total current in the primary of T1 and the reactive diode current for a 125 va, 45° inductive load. For the inductive load, the currents are reduced. The average diode current, for example, is estimated to be 4.5 ma, and the peak current is 200 ma. The output filter is capacitive, and with a resistive external load, the power converters see a capacitive load. With an inductive output load, the power converters see a load that more nearly approaches unity power factor. Since the output filter is capacitive, it is assumed that it was designed in anticipation of an inductive inverter load.

Figures 47 and 48 illustrate the difficulties of estimating worst-case conditions for the power converters. The operating conditions are determined by the external load characteristics, and these are not specified except for magnitude.

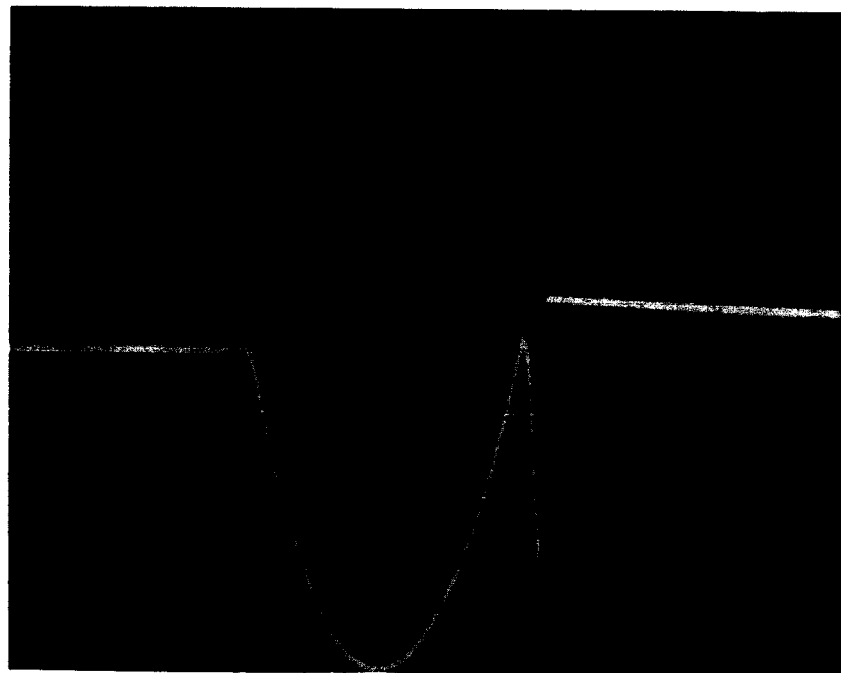
The static inverter voltage regulation loop controls the average three-phase output voltage, but not the balance between the three phases. There is no feedback control on the output voltage balance as determined by the power converter and output circuit components. Initially, the breadboard model of the static inverter would not meet the voltage imbalance specifications, and it was necessary to "trim"



Primary Winding Current

Vertical Scale: 1 a per div.

Horizontal Scale: 0.2 ms per div.

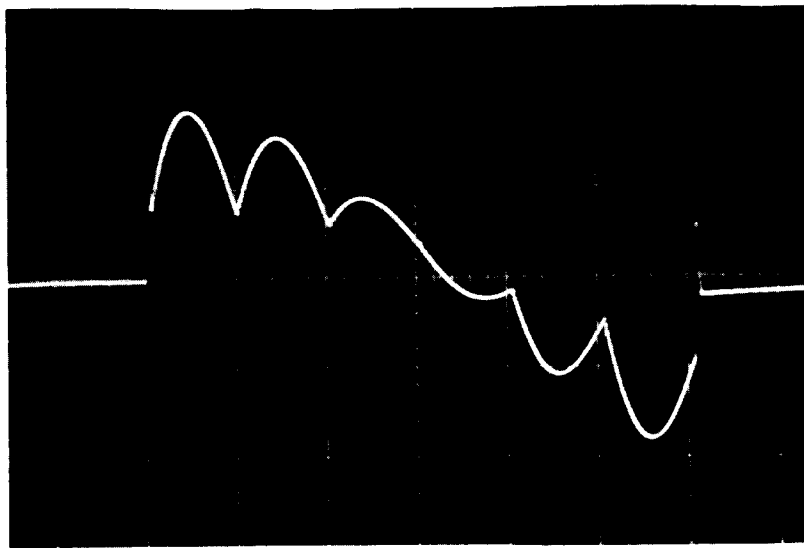


Reactive Diode Current

Vertical Scale: 0.2 a per div.

Horizontal Scale: 50 μ s per div.

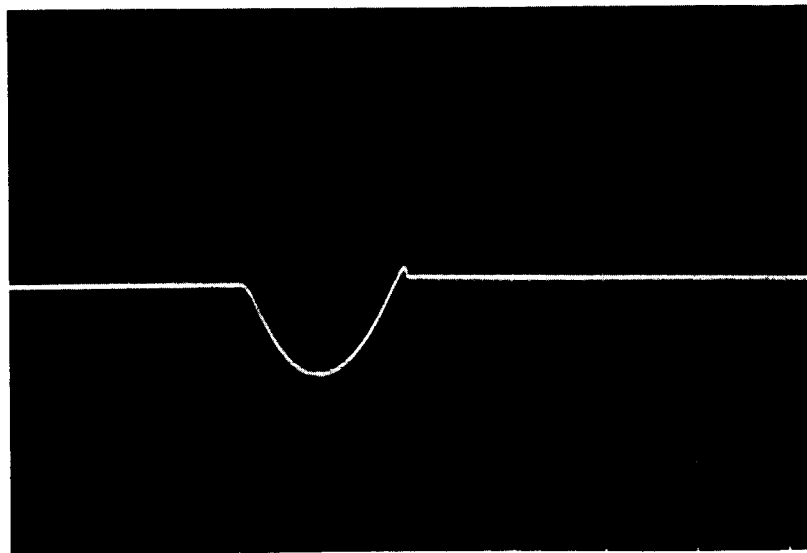
Figure 47. Power Converter Transformer Primary Winding Current and Reactive Diode Current for 125 VA Resistive Load



Primary Winding Current

Vertical Scale: 1 a per div.

Horizontal Scale: 0.2 ma per div.



Reactive Diode Current

Vertical Scale: 0.2 a per div.

Horizontal Scale: 50 μ s per div.

Figure 48. Power Converter Transformer Primary Winding Current and Reactive Diode Current for 125 \angle +45° VA Load

the turns ratios of two of the power converter transformers. T5 and T6 were trimmed to more closely approximate the characteristics of T1 - T4 by adding primary turns in a negative H direction, and a satisfactory balance was achieved. The inverter voltage balance characteristics can undoubtedly be improved over the breadboard characteristics by a careful initial selection of transformers.

3.3.4.10 Output Circuit (Element 58)

Schematic: Figure 49.

Function: (1) Provide the interconnection of the 18 power converter secondary windings such that a 3-phase, 400 cps output voltage waveform is generated.

(2) Provide filtering for attenuating the harmonics of the fundamental 400 cps component.

(3) Provide power factor correction for inductive loads.

Input: 18 square wave voltages with three different magnitudes and six different phases.

Load: (1) Inverter output load.
(2) Overcurrent detection circuit.
(3) Voltage error detection circuit.

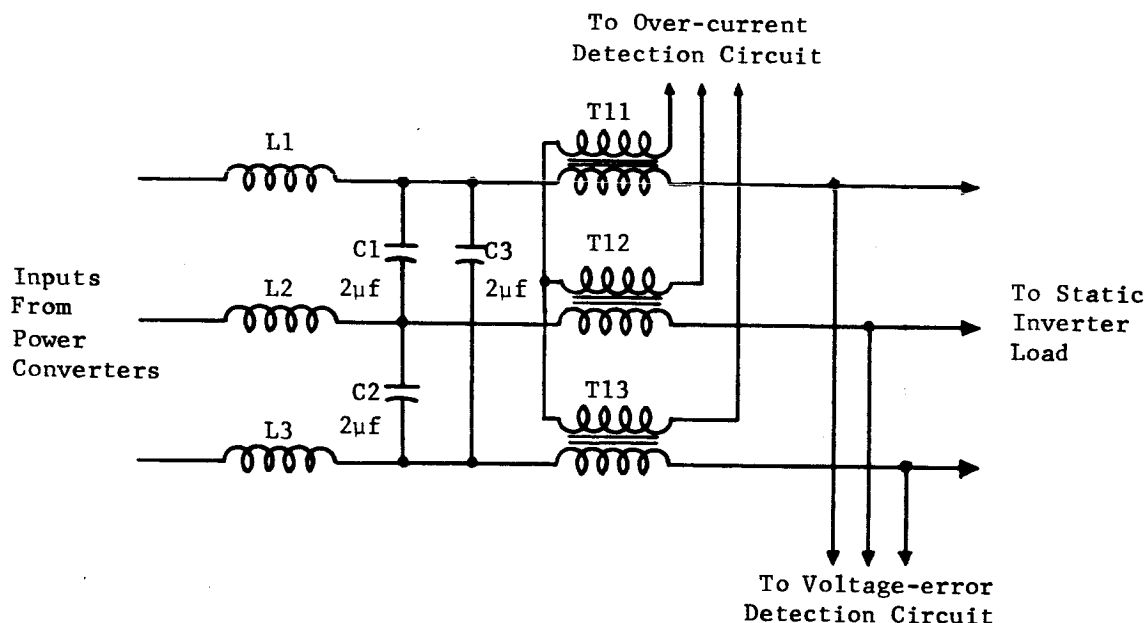


Figure 49. The Output Circuit

- Attributes: (1) Average three-phase output voltage.
 (2) Output voltage distortion.
 (3) Output voltage imbalance.
 (4) Output phase imbalance.

Remarks: The interconnections between the eighteen secondary windings on the power converter transformers to provide a 3-phase, 400 cps output has been described [Ref. 1]. The resulting stepped waveform is analyzed, and the effect of the output filter on output distortion and voltage and phase imbalance is examined in detail in Section 3.3.1.4. The component stress analysis of Section 3.3.1.3 illustrates that all components in the output circuit are applied within their rated capabilities.

3.3.4.11 Voltage Error Detection Circuit (Element 59)

Schematic: Figure 50.

Function: To supply a control winding current to the magnetic amplifier that is proportional to the output voltage error.

Input: The three-phase, 115 vac inverter output voltage.

Load: Magnetic amplifier control winding; approximately 0.25 ma maximum.

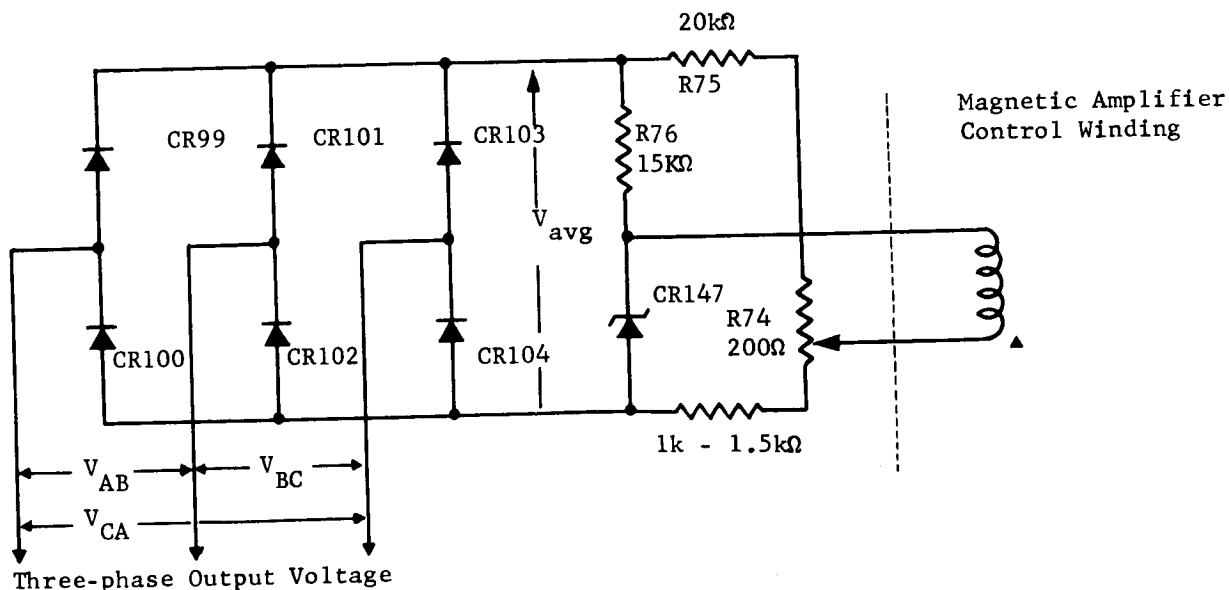


Figure 50. Voltage Error Detection Circuit R73

Attributes: Output current to control winding.

Remarks: The voltage error detection circuit has been described and analyzed [Ref. 2]. The functional operation of the circuit has been described [Ref. 1] and the component stress analysis of Section 3.3.1.3 of this report shows that the stress on any component is well within its rated capabilities. As part of the voltage regulation loop, the voltage error detection circuit has been included in the analysis of the voltage control loop in Section 3.3.2.2. Sensitivities of the average three phase voltage output to the parameter values of the voltage error circuit components for different values of control loop gain were computed and also reported in that section.

3.3.4.12 Overcurrent Detection Circuit (Element 60)

Schematic: Figure 51.

Function: Provide a control current to the magnetic amplifier in the event of excessive output current so as to reduce the magnetic amplifier modulation and limit the output current.

Input: (1) 20 vdc from the regulated 20 volt supply.
(2) Voltages proportional to inverter output line currents via transformer T11 - T13.

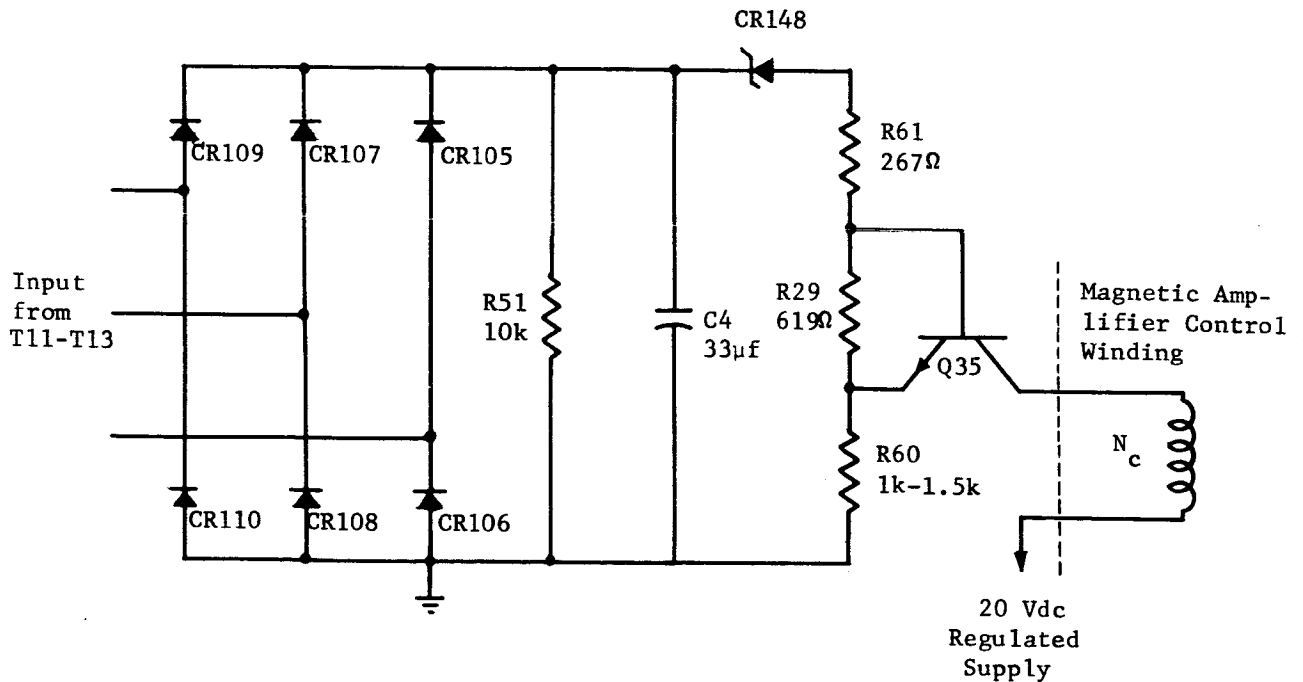


Figure 51. Overcurrent Detection Circuit

Load: Less than 20 ma in the magnetic amplifier control winding.

Attributes: Impedance to the magnetic amplifier control-winding current.

Remarks: The primaries of the transformers in the overcurrent detection circuit (OCD) have a negligible impedance to the primary current, i.e., the static inverter output current; the time constant of the filter on the output of the three-phase rectifier is sufficiently large to cause the OCD circuit to be equally sensitive to an excessive current in one or all output phases; and the average three-phase rectifier output voltage is 6.05 volts per rms ampere of line current [Ref. 2]. The threshold value of line current, i.e., the line current at which the three-phase rectifier voltage is 8.4 volts, is 1.4 rms amperes. The threshold level of the OCD circuit has been discussed in connection with an observed failure mode in the magnetic amplifier output circuit [Ref 2]. The conclusions concerning the failure mode have since been modified and are discussed in detail in Section 3.3.4.15 of this report, but the conclusions concerning the OCD circuit remain valid. The threshold level of the OCD circuit is such that the static inverter may fail due to certain excessive loads.

With reference to Figure 51, assume that $R_{60} = 1 \text{ k}\Omega$, i.e., its lowest specified value; that the base emitter threshold voltage of Q35 is 0.45 volts; and neglect any saturation effects in T11 - T13. For these conditions, the current through R29 must be

$$I_R = \frac{.45 \text{ v}}{619 \Omega} = 0.728 \text{ ma}$$

before the OCP circuit could have any influence on the inverter output current. This nominally corresponds to a three-phase rectifier voltage of

$$V_R = 8.4 \text{ v} + (.728 \text{ ma}) (1.89 \text{ k}\Omega) = 9.8 \text{ volts}$$

where 1.89 k Ω is the series resistance of R29, R60 and R61; and to an output line current of

$$I_L = \frac{9.8 \text{ v}}{6.05 \text{ v/amp.}} = 1.62 \text{ amps}$$

where 6.05 is the OCD rectifier voltage per ampere of line current. If it is assumed that the threshold value of V_{BE} for Q35 is 0.8 volts, then the nominal value of line current is increased to

$$I_L = \frac{8.4 \text{ v} + \frac{.8 \text{ v}}{.619 \text{ k}\Omega} (1.89) \text{ k}\Omega}{6.05 \text{ v/amp}} = 1.79 \text{ amps.}$$

This value corresponds closely to the experimental value of line current for which the OCD circuit begins to influence the inverter output that was previously reported [Ref. 2].

The over-current protection effectiveness can be increased by reducing the value of line current at which the OCD circuit begins to limit the inverter output. This can be accomplished by reducing the zener breakdown of CR148, reducing R60, and/or increasing R29. This modification could eliminate the failure mode discussed in Section 3.3.4.15.

Once the OCD circuit becomes effective, it protects the static inverter from damage due to overloads by quickly reducing the magnetic amplifier modulation and thus the output voltage. As the external load is increased to a short circuited output, the inverter goes into a limit cycle operation.

3.3.4.13 20-Volt dc Regulated Supply (Element 61)

Schematic: Figure 52.

Function: Provide a regulated 20-volt supply to the magnetic amplifier driver circuit and to the overcurrent detection circuit.

Input: Unregulated 25 - 30 vdc inverter input voltage.

Load: Less than 97 ma (average) at 20 volts to elements 60 and 62.

Attributes: (1) Output voltage.
(2) Output voltage ripple.
(3) Output voltage regulation.

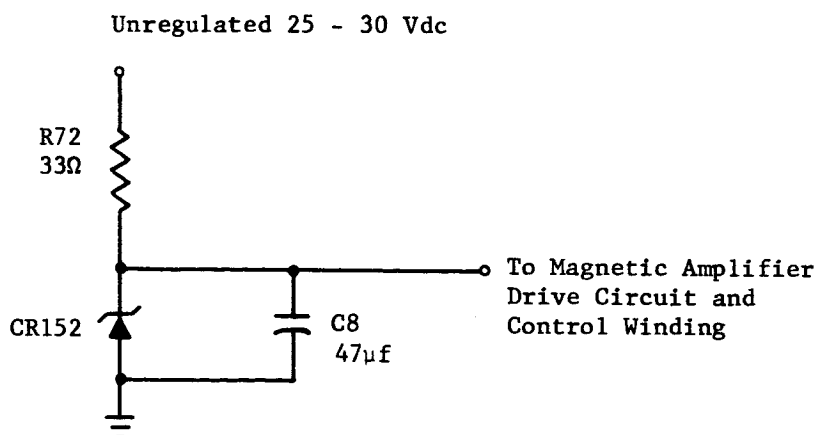


Figure 52. 20 Vdc Regulated Supply

Remarks: The 20 vdc regulated supply will function as a low impedance, zener voltage source for all expected load and environmental conditions. The output voltage remains between 18.5 and 21.5 volts for output currents from zero to more than 100 ma which is satisfactory for the circuits supplied. The capacitor filter, C8, maintains the output voltage ripple at a negligible level.

The component stress analysis of Section 3.2.1.1 concludes that C8 and R72 are within their rated capabilities. Caution is advised with respect to CR152, however. This zener diode is nominally rated to dissipate 10 watts at 25°C and, in this application, will dissipate approximately 6.7 watts at worst-case conditions. The worst-case conditions correspond to inverter operation in an overload mode such that the magnetic amplifier is completely turned off, and the current supplied to the OCD circuit is negligible. Since the manufacturer of CR152 does not recommend a derating schedule, it cannot be concluded that the power dissipation capability of CR152 will be satisfactory at 100°C. It is recommended that a higher nominal wattage rating be specified for CR152, e.g., a power dissipation rating at 25°C of 15 watts.

3.3.4.14 Magnetic Amplifier Driver Circuit

3.3.4.14.1 Original Version (Element 62)

Schematic: Figure 53

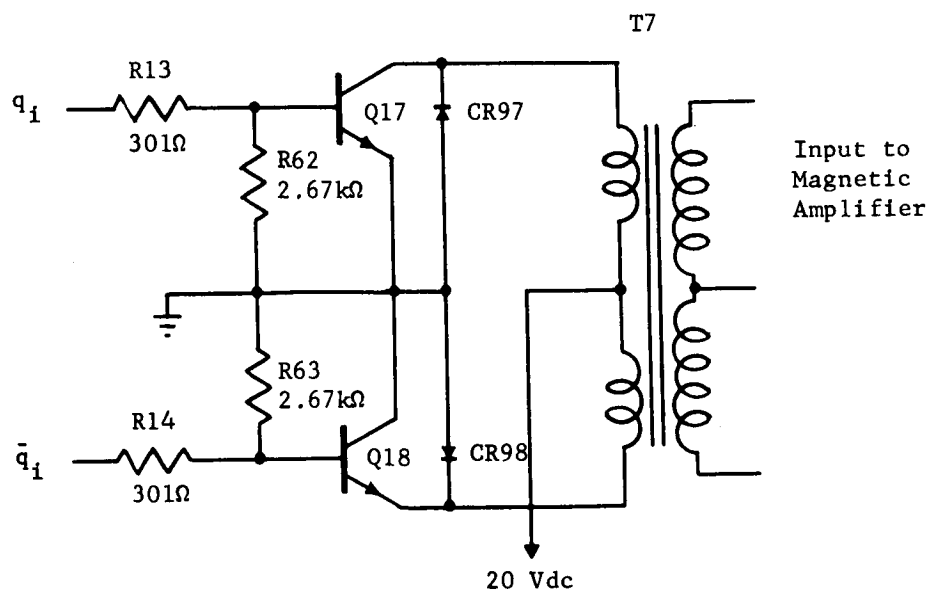


Figure 53. Magnetic Amplifier Drive Circuit

Function: Provide two regulated complementary 4.8 kc square wave inputs to the magnetic amplifier.

Inputs: (1) 20 vdc from the regulated 20 v supply at less than 100 ma.
(2) two complementary, positive-going square waves from the frequency countdown circuit.

Load: Magnetic amplifier; 2 watts peak.

Attributes: Output voltage amplitude.

Remarks: The design of the magnetic amplifier circuit was concluded to be adequate [Ref. 2], and subsequent analyses with improved component data have confirmed those conclusions. Each component is applied within its rated capabilities, and the switching transistors are driven into saturation by the minimum base drive current.

It was pointed out in Sections 3.3.4.7 and 3.3.4.8 that the minimum base current available to drive the TPA transistors was inadequate to insure saturation. Consequently, a modification was suggested that provided adequate base drive to the TPA transistors and also increased the reliability of the system. Because of the similarity between the TPA's and the magnetic amplifier drive circuit, a similar modification was considered and concluded to be desirable for the magnetic amplifier drive circuit. The modified version is considered in the following section.

3.3.4.14.2 Modified Version (Element 62M)

Schematic: Figure 54.

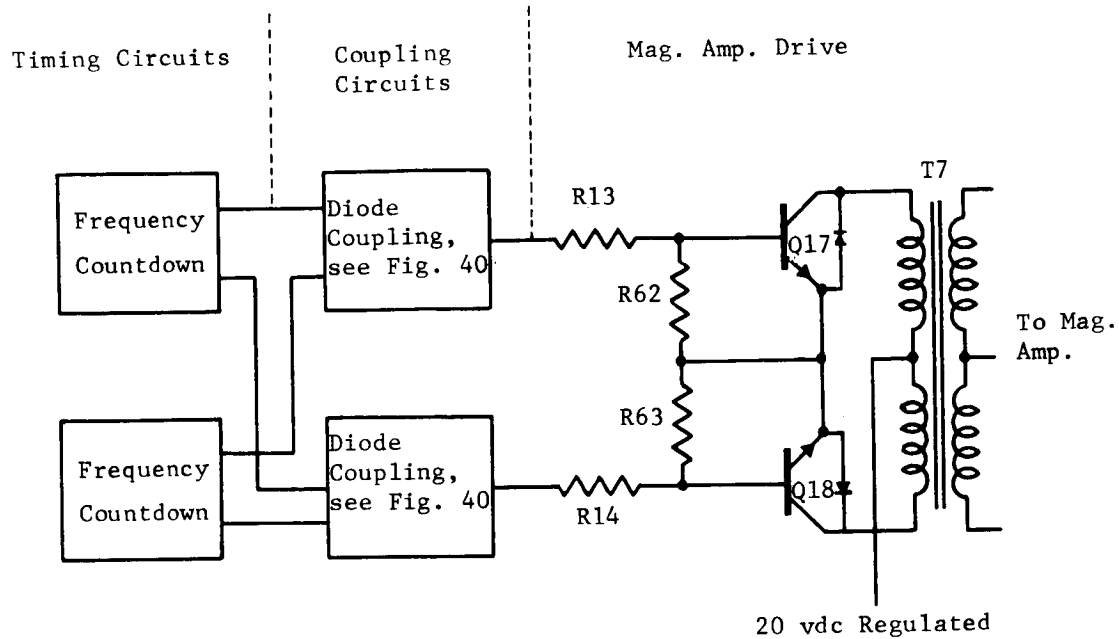
Function: Same as original version.

Inputs: Same as original version.

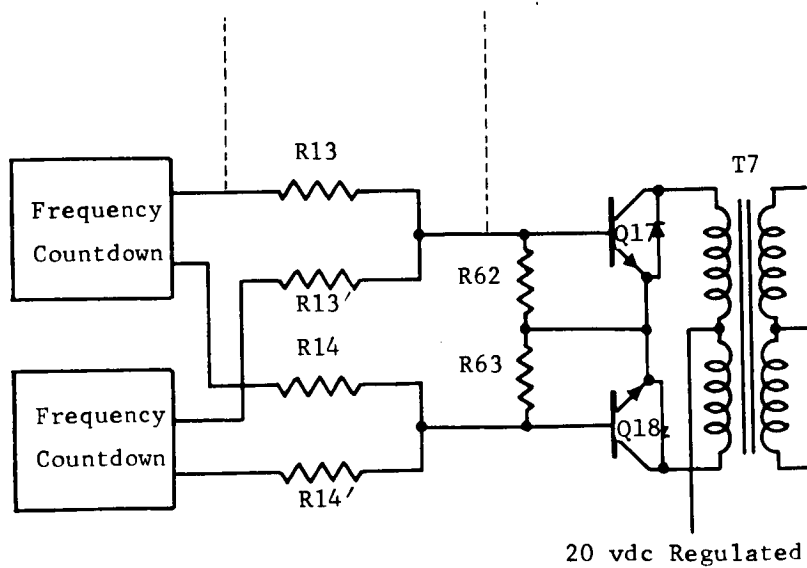
Loads: Same as original version.

Attributes: Same as original version.

Remarks: This modification is similar to the TPA modification discussed in Section 3.3.5.8.2. The original diode coupling circuits are replaced with resistor networks, and the two timing generators are resistively coupled to the magnetic amplifier drive circuit. In the original version, R13 and R14 are 301 Ω resistors; and in the modified version, R13 and R13', R14 and R14' constitute the modified coupling circuits (Elements 32 and 33) and are 412 Ω resistors. The modified circuit has been analyzed [Ref. 3] and provides adequate base drive to Q17 and Q18, adequate isolation between the two timing generators, and increased reliability.



Original Version



Modified Version

Figure 54. Illustration of the Mag. Amp. Drive Circuit and Coupling Circuit Modification

3.3.4.15 Magnetic Amplifier Circuit (Element 63)

Schematic: Figure 55

Function: Amplify the voltage error signal and modulate the voltage regulator so as to reduce the output voltage error.

Inputs: (1) Two complementary square waves at 12 volts from the magnetic amplifier driver circuit.
(2) Control winding current from the voltage error detection circuit.
(3) Control winding current from the overcurrent detection circuit.

Loads: A maximum of 2.68 amps at 3.9 volts to the voltage regulator circuit.

Attributes: (1) Output voltage.
(2) Output current.
(3) Output modulation.

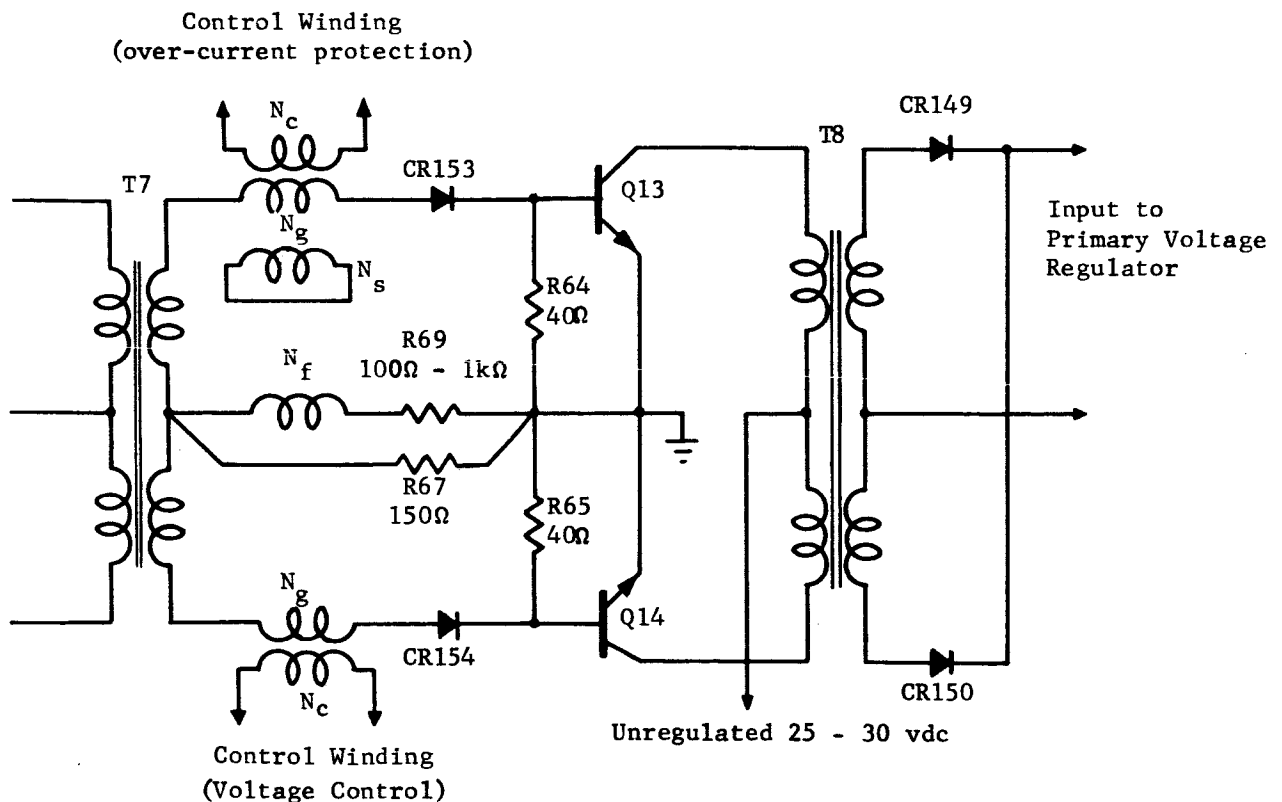


Figure 55. Magnetic Amplifier Circuit

Remarks: The magnetic amplifier has been previously described [Ref. 1] and analyzed [Ref. 2]. Experimental efforts have been very useful in a continuing study of the magnetic amplifier, and previous conclusions have been either substantiated or modified by the experimental program.

The magnetic amplifier transfer curve has been described [Ref. 1], and the measured transfer curve for the magnetic amplifier used in the static inverter is shown in Figure 56. To obtain this data, the control current on the abscissa was measured in the voltage control winding of the magnetic amplifier, but the results should be identical for current in either control winding or for the sum of the currents in both control windings. Figure 56 demonstrates the negligible effect of temperature on the transfer characteristics and the effect of the positive feedback

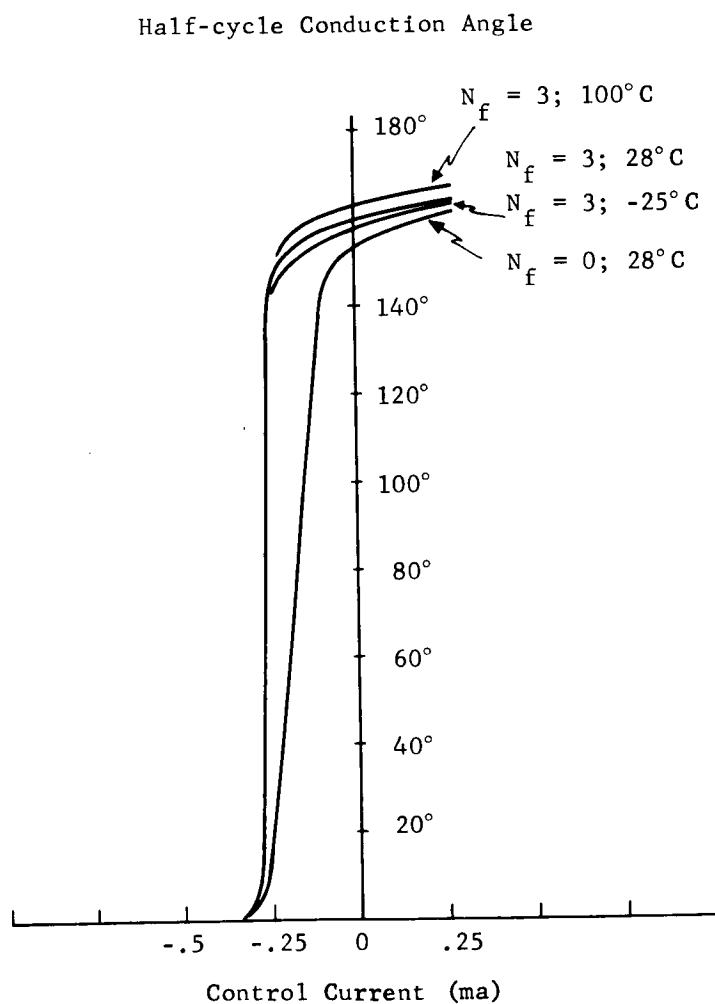


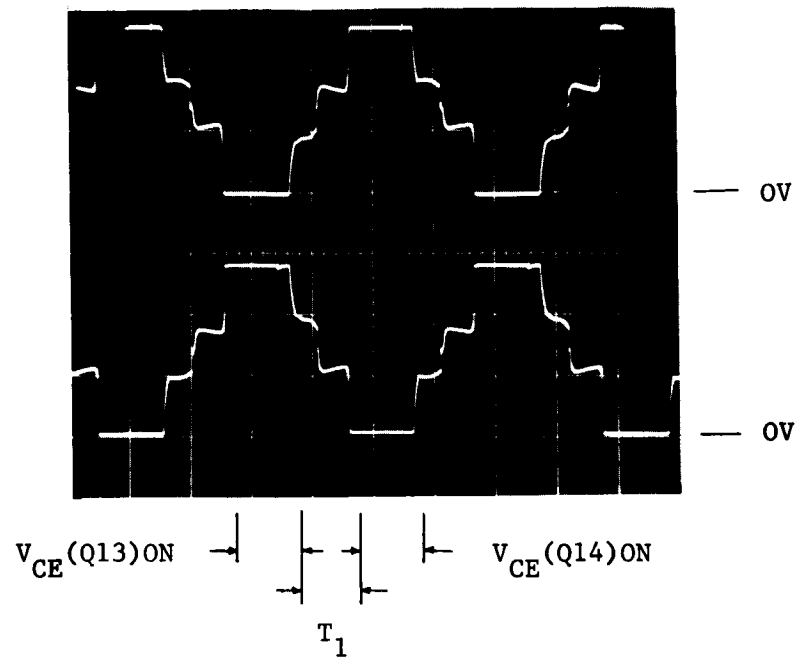
Figure 56. Transfer Curves for the Magnetic Amplifier Circuit

due to N_f . Increasing the positive feedback from zero increases the gain, i.e., the slope of the transfer curve, of the magnetic amplifier to the point of instability. Experimentally, the magnetic amplifier has been observed to become unstable over a small portion of the transfer curve as feedback was increased. The unstable region also increased to cover most of the reset region as the feedback was increased further. The positive feedback is determined by selecting a value of N_f and R69 that causes the inverter to have the desired voltage regulation. Section 3.3.3.2 of this report discusses criteria for adjusting the feedback loop gain, i.e., the magnetic amplifier positive feedback. Experimentally, the loop gain has been increased by varying N_f and R69 until the average three-phase output voltage increased with increasing load, and further until the static inverter became unstable.

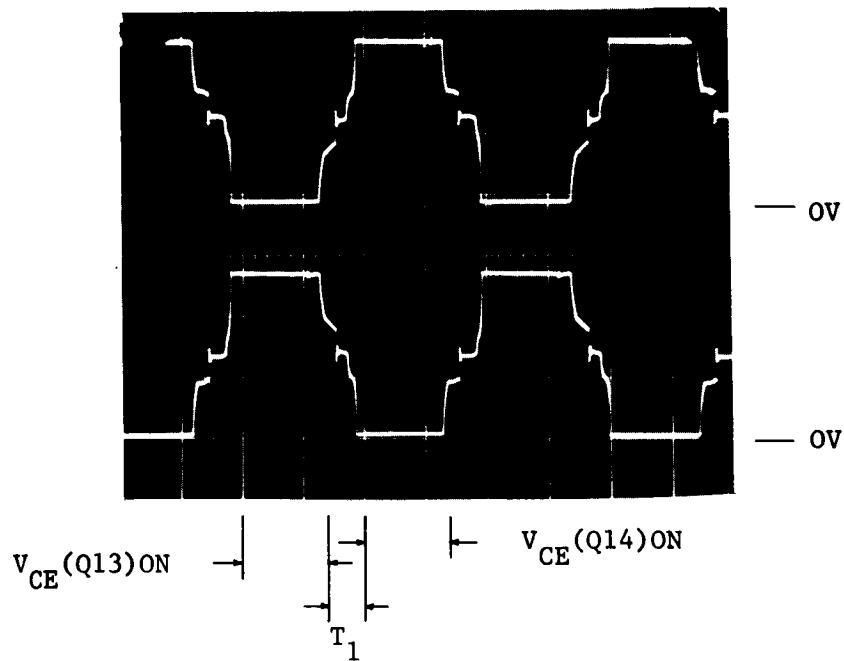
From the transfer characteristics of Figure 56, it is observed that the magnetic amplifier does not become 100% modulated, i.e., the half-cycle conduction angle is less than 180° , for zero control winding current. This is probably due to the roundness of the HyMu magnetic amplifier cores. It is observed that for the core material used, residual flux density is approximately 87% of the saturation flux density, and the magnetic amplifier operating point at zero control current is approximately 89% of 180° . Therefore, roundness in the magnetic amplifier can account for the less than 100% modulation.

Section 3.0 of Reference 2 discussed a frequently observed failure in the magnetic amplifier circuit. It was noted that as the load on the static inverter was increased beyond rated load, the switching transistors in the magnetic amplifier output stage, Q13 and Q14, would consistently fail. In Reference 2, the observed failures were recorded and discussed in considerable detail, and it was concluded that the power dissipation capabilities of Q13 and Q14 were inadequate. Further consideration of this failure has led to additional conclusions that are discussed in the following paragraphs. It is emphasized that this failure has not occurred when the inverter was operating in a normal mode, but only when the inverter was supplying a load in excess of rated load. As the load on the inverter is further increased, the OCP loop becomes effective to reduce the magnetic amplifier modulation and protect the inverter circuitry.

Figure 57 shows the collector-emitter voltage waveforms (V_{CE}) for Q13 and Q14 for one-half and full rated load conditions. The ON period for each transistor is shown in the figure and corresponds to the period that V_{CE} is approximately zero volts. The period T_1 corresponds to the period that neither transistor is ON, and



125 \angle 45° VA Balanced Load



250 \angle 45° VA Balanced Load

Vertical Scales: 20 V per div.

Horizontal Scales: 50 μ s per div.

Figure 57. Collector-Emitter Waveforms of Q13 and Q14

decreases as the load on the static inverter is increased. The power dissipated by Q13 or Q14 is given by

$$P_d = \frac{1}{T} \int_0^T V_{CE} I_C dt. \quad (27)$$

The use of this relationship is difficult for the waveforms of Figure 57, but as the modulation of the magnetic amplifier increases, i.e., as T_1 approaches zero, Equation (27) can be closely approximated by

$$P_d = [(V_{CE} I_C)_{ON} T_{ON} + (V_{CE} I_C)_{OFF} T_{OFF} + \int_{Sw.Time} V_{CE} I_C dt] \frac{1}{T}, \quad (28)$$

where the last term accounts for the power dissipated during switching times. Normally, this term is negligible and T_{ON} and T_{OFF} become $T/2$. Neglecting the last term in Equation (28), the worst-case power dissipation computed for Q13 or Q14 is within their rated capacity. It is probable that the switching term in Equation (28) is not negligible in this application and is the term responsible for the observed failures. The gain bandwidth product (f_T) for Q13 and Q14 is specified by the manufacturer to be within 1 Mc and 6 Mc. If f_T is 1 MC, for example, and h_{FE} is 100 which is a probable value, then f_β can be approximated from

$$f_\beta \approx f_T/100 \quad (29)$$

to be approximately 10 kc which is much too low for this application. One would expect the switching term in Equation (28) to become large and the transistor to fail. A satisfactory solution to this problem would be to screen the transistors to ascertain that $f_T \geq 5$ Mc. f_β can also be increased by reducing h_{FE} , but a minimum value of h_{FE} must also be assured for satisfactory operation.

As the external static inverter load is increased, the modulation of the magnetic amplifier increases until T_1 in Figure 57 approaches zero. Because of the relatively slow switching capabilities of Q13 and Q14, it is probable that both Q13 and Q14 would be ON at the same time, i.e., T_1 would become negative, and failure would follow. In observing this failure, the waveforms of Figure 57 become square waves and V_{CE} during the ON period begins to increase rapidly. This is indicative of rapidly increasing collector current due to thermal run-away.

The component stress analysis of Section 3.3.1.3 shows the adequate capabilities of the static inverter components, including Q13 and Q14, for the normal mode of operation.

The dynamic performance of the magnetic amplifier is also of concern. In Section 3.3.3.2, the voltage control loop is discussed in detail and it is shown that the magnetic amplifier output, i.e., its duty cycle, is described by

$$\frac{d\tau}{dt} + \frac{R_e}{K'_\phi} \tau = C_1 + C_2 V, \quad (30)$$

where

τ = pulse width of magnetic amplifier output,

R_e = resistance of equivalent control circuit,

K'_ϕ = a magnetic amplifier core parameter descriptive of the slope of the transfer curve.

C_1 = constant determined by circuit parameters,

C_2 = constant determined by circuit parameters, and

V = rms value of output voltage into a balanced load.

In modeling the voltage regulation loop (see Section 3.3.3.2), it was necessary to evaluate the constants in Equation (30). For steady-state conditions, i.e., $d\tau/dt = 0$, R_e in Equation (30) is canceled and the steady-state value of τ is

$$\tau_{ss} = C_3 + K'_\phi (C_4 + C_5 V). \quad (31)$$

Using computed values of the constants, Equation (31) agrees very closely with the experimentally observed transfer characteristics. However, for transient operation the experimentally observed value of R_e/K'_ϕ , i.e., the reciprocal of the time constant of the magnetic amplifier, did not compare favorably with the computed value. Since R_e could not be measured directly for comparison, the entire quantity, R_e/K'_ϕ , was evaluated experimentally. Figure 58 is a sketch of the magnetic amplifier output waveform. By simulating a step function in output voltage V , the ON time of the magnetic amplifier changes from a value τ_i to τ_f . The change should follow the first order response of Equation (30). Figure 59 is an oscillogram showing the change in τ at 2.5 ms intervals in response to a simulated step change in V with the control loop open circuited. The 2.5 ms displays were obtained by externally triggering the oscilloscope with a 400 cps signal from the static inverter. From oscillograms such as this, the magnetic amplifier transient response was plotted on semi-log scale as shown in Figure 60 for the different magnetic amplifier feedback (N_f) conditions. The ordinate is interpreted as follows. In response to a step function in V , solutions to Equation (30) are of the form

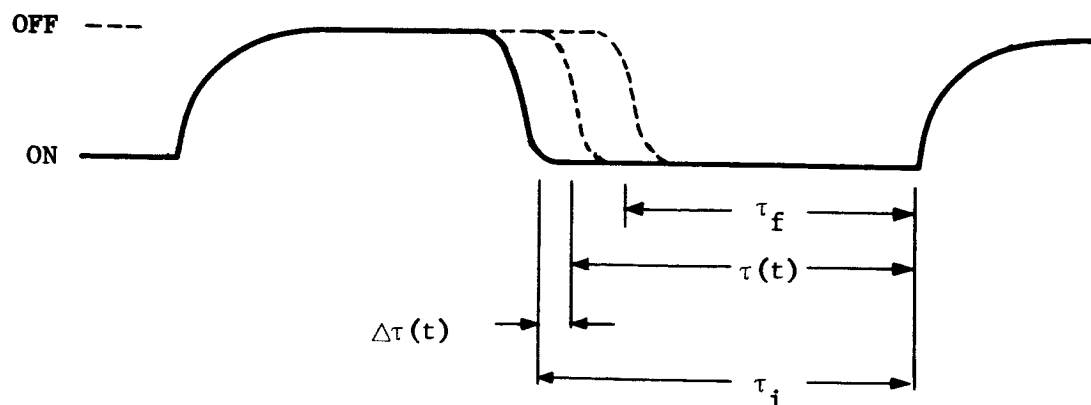


Figure 58. Magnetic Amplifier Output Waveform Defining τ_f , τ_i , and $\tau(t)$

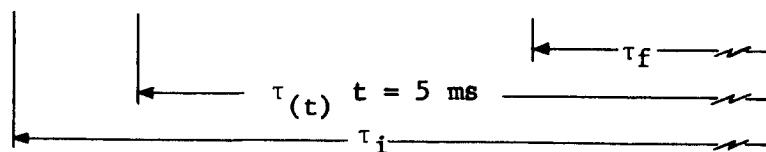
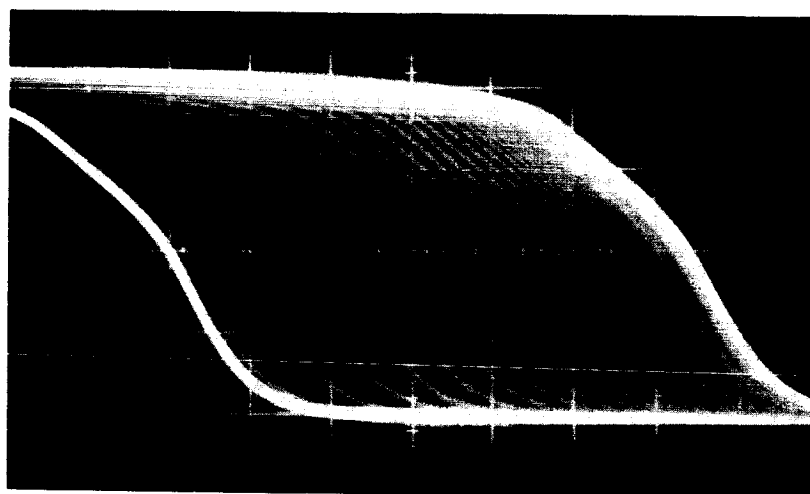


Figure 59. Oscilloscope Showing $\Delta\tau$ at 2.5 ms Intervals

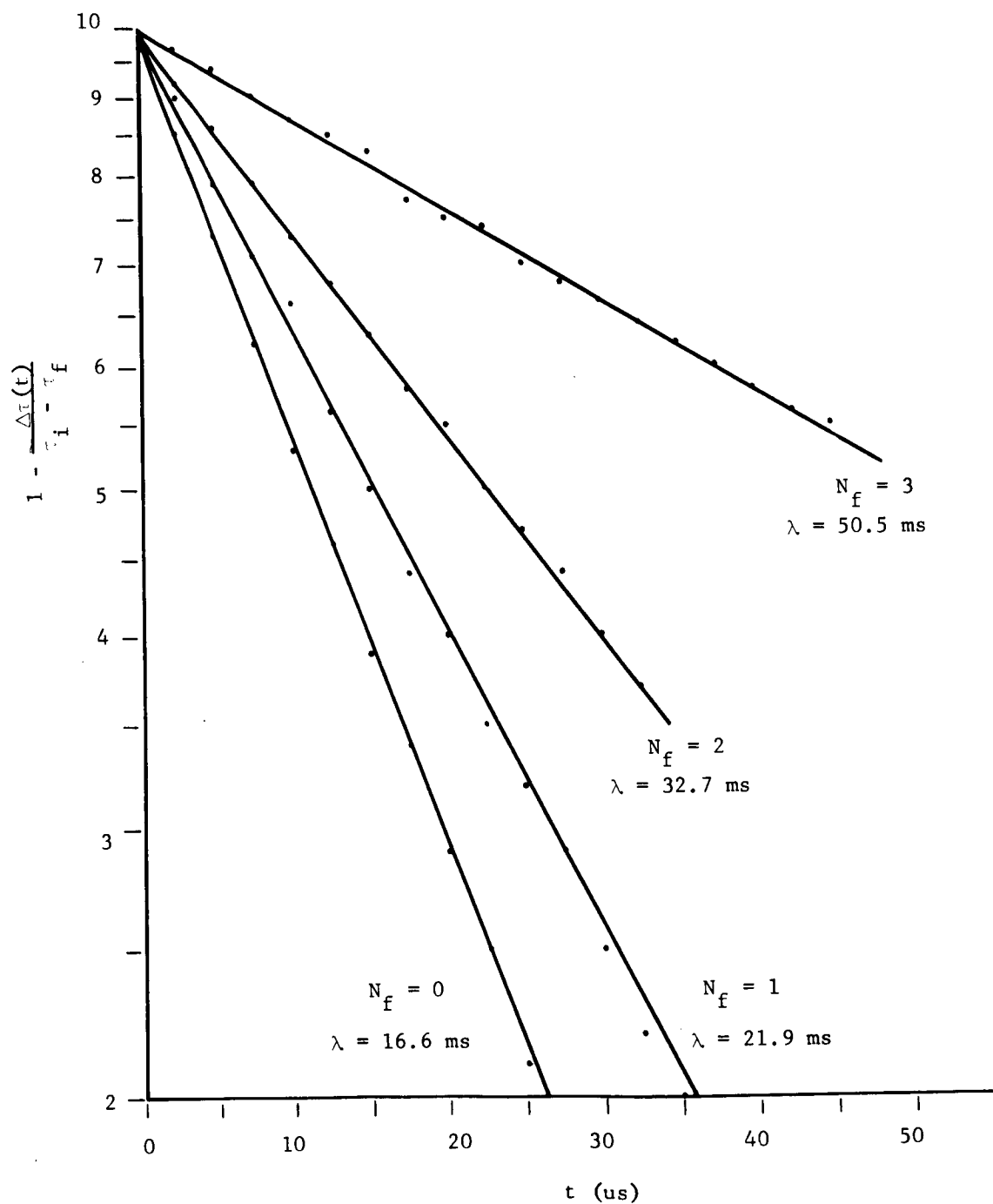


Figure 60. Magnetic Amplifier Time Constant Measurements

$$\tau(t) = \tau_i - (\tau_i - \tau_f) (1 - e^{-\lambda t}) \quad (32)$$

where $\lambda = K'_\phi/R_e$ and τ_i and τ_f are the initial and final values of τ . From Equation (32), one can write

$$-\lambda t \log_{10} e = \log_{10} \left[1 - \frac{\Delta\tau(t)}{\tau_i - \tau_f} \right] \quad (33)$$

where $\Delta\tau(t)$ is defined in Figure 58 as $\tau_i - \tau(t)$. Therefore, the slopes of the plots in Figure 60 are $-\lambda \log_{10} e$ for the different values of N_f and the straight lines illustrate that the response is first order. The value of K'_ϕ/R_e for $N_f = 3$ is 16.6 ms. Values of the time constant for other values of N_f are also shown in Figure 60.

In Reference 1, it was pointed out that the shorted turns (N_s) on the magnetic amplifier functioned to slow down its response. This was verified experimentally, but not analyzed in detail.

3.3.4.16 Primary Voltage Regulator

Schematic: Figure 61.

Function: Regulate the average static inverter three-phase output voltage by pulse modulating the inverter input voltage to control the dc voltage supplied to the power converters.

Inputs: (1) A modulated square wave from the magnetic amplifier.
(2) 28 vdc from the unregulated input voltage source.

Load: A maximum of 250 va of controlled dc at 19 to 21 volts.

Attributes: (1) Output voltage.
(2) Output voltage ripple.

Remarks: The design of the voltage regulator circuit has been analyzed and it was concluded that, except for excessive ripple current in C5, the design was adequate [Ref. 2]. Since that analysis, improved component data and more realistic assumptions resulting from breadboard experience have provided a more accurate design analysis, and several of the earlier conclusions have been modified. In particular, it cannot be concluded from published characteristics that base drive is adequate for saturating the voltage regulator transistor switches. It is, however, concluded that a transistor switch with insufficient gain to assure saturation would be rare.

Except for the small demands of the timing section and the 20 vdc regulated supply, the input current to the static inverter passes through the primary voltage regulator. Assuming an efficiency of 80% for the power section of the inverter, the maximum average current in the regulator is estimated to be

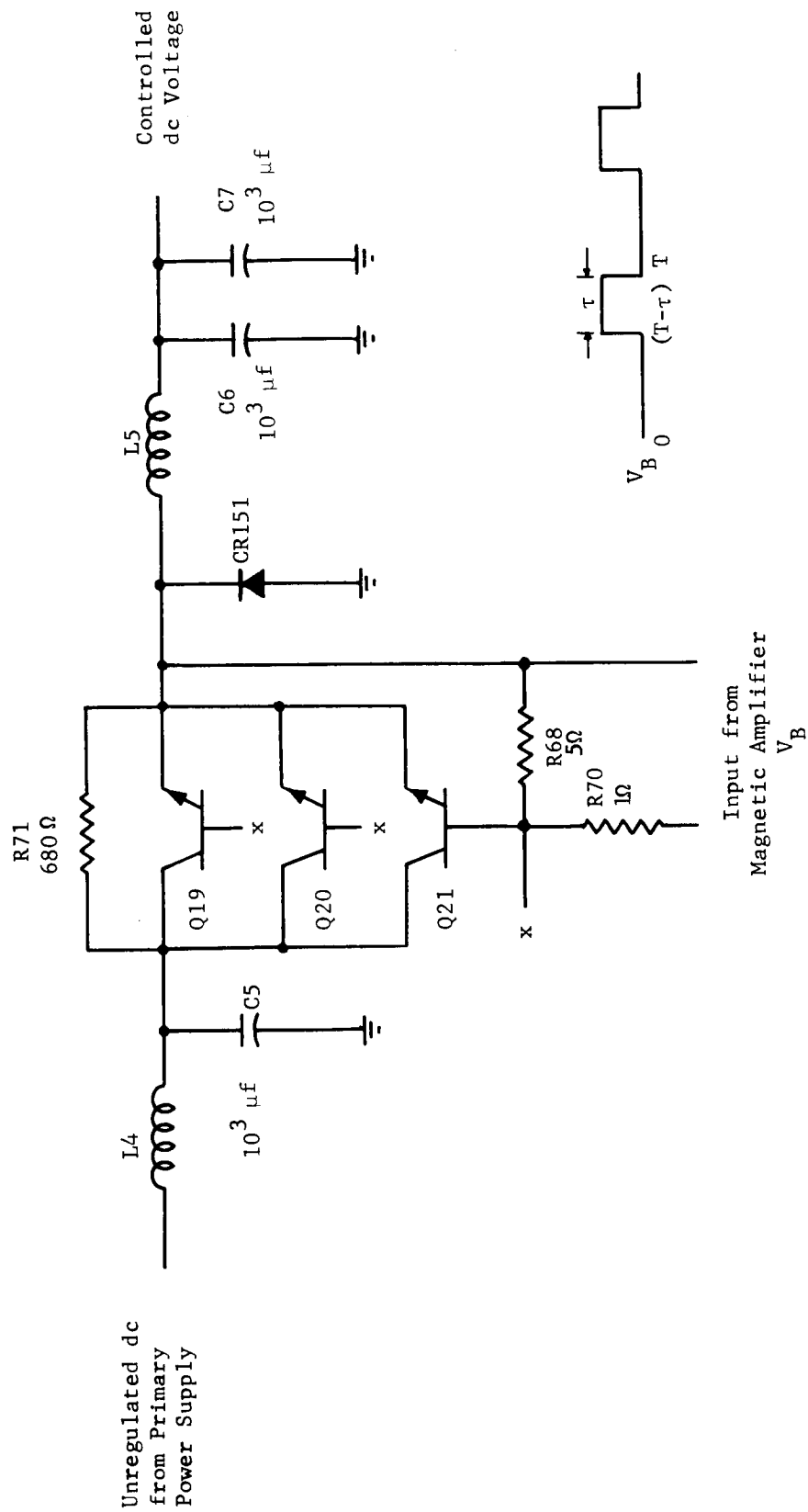


Figure 61. Primary Voltage Regulator

$$I_{in} \text{ (max avg.)} = \frac{250 \text{ va}}{(25\text{v}) (.8)} = 12.5 \text{ a.}$$

If it is further assumed that the voltage regulator is ON 80% of the time at full load conditions, the maximum peak regulator current will be

$$I_{peak} = \frac{12.5}{.8} = 15.5 \text{ amps}$$

Assuming the three parallel transistor switches to be perfectly balanced, each transistor must conduct a maximum current of

$$I_{C(Q19 - Q21)} = \frac{15.5 \text{ a}}{3} = 5.2 \text{ amps}$$

The base drive current supplied to the voltage regulator circuit by the magnetic amplifier output is estimated to have a minimum value of 1.27 amperes. This assumes a worst-case input voltage to T8, transformer (T8) winding resistances 10% above measured values, a maximum value for R70, .7 v forward drop for CR149 and CR150, a base-emitter drop of 1.1 v for Q19 - Q21, and neglects core losses in T8. Subtracting the maximum current expected in R68, the total base current in Q19 - Q21 will be a minimum of

$$I_{B(min)} = 1.27 \text{ a} - 0.23 \text{ a} = 1.04 \text{ a,}$$

and the minimum base current per transistor will be

$$I_{B(Q19 - Q21)} = 0.34 \text{ a.}$$

Consequently, each transistor must have a minimum gain of

$$h_{FE} = \frac{5.2 \text{ a}}{.34 \text{ a}} = 15.3.$$

The minimum gain specified by the manufacturer is 10, but it is concluded from the published data brochures that a transistor with a gain less than 20 at the conditions of interest would be rare. It is recommended, however, that the voltage regulator transistors be screened to ascertain a minimum value of h_{FE} of 20 at $V_{CE} = 1 \text{ v}$ and $I_C = 5 \text{ amperes}$. The increase over 15.3 will provide a safety margin for the uncertainties involved in the preceeding assumptions. These assumptions were necessary to complete the analysis and are considered to be realistic.

In Reference 2, it was estimated that the rms ripple current in C5 would be 6.4 a, and it was reported to have been observed at 5.3 a. Numerous approximations are involved in estimating the ripple current in C5, and there is considerable un-

certainty in the final estimate. It is certain, however, that the ripple current is excessive compared to the rated value of 1.8 a, and it is recommended that this problem be minimized by taking steps to decrease the equivalent series resistance in the C5 path. It was also pointed out in Reference 2 that the ripple current in CR was not independent of the inverter input voltage source characteristics, and there are no specifications descriptive of the input voltage source.

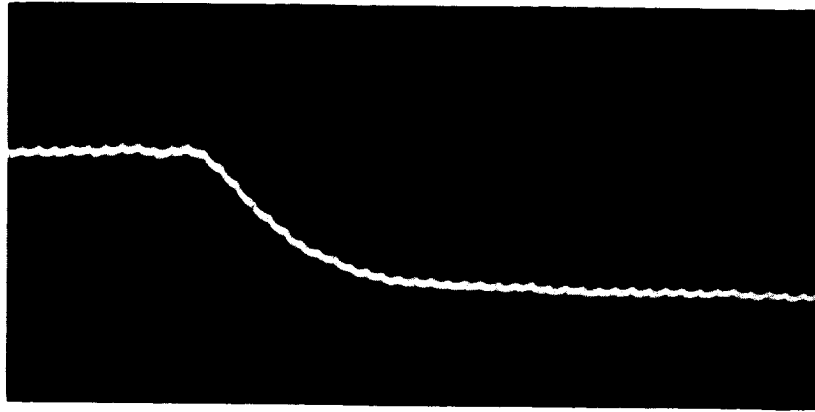
In all other respects, the design of the primary voltage regulator is concluded to be adequate. The component stress analysis in Section 3.3.1.3 shows the remaining components to be applied within their rated capabilities.

The transient performance of the primary voltage regulator is also of interest. It is pointed out in Section 3.3.3.2 that the primary voltage regulator along with the six power converters and the output circuit form the forward portion of the voltage regulator loop. The equation describing the transient response of the forward portion of the loop is given in Section 3.3.3.2 as

$$\frac{d^2V}{dt^2} + A_1 \frac{dV}{dt} + A_0 V = B_0 + B_1 V_{in} \tau . \quad (34)$$

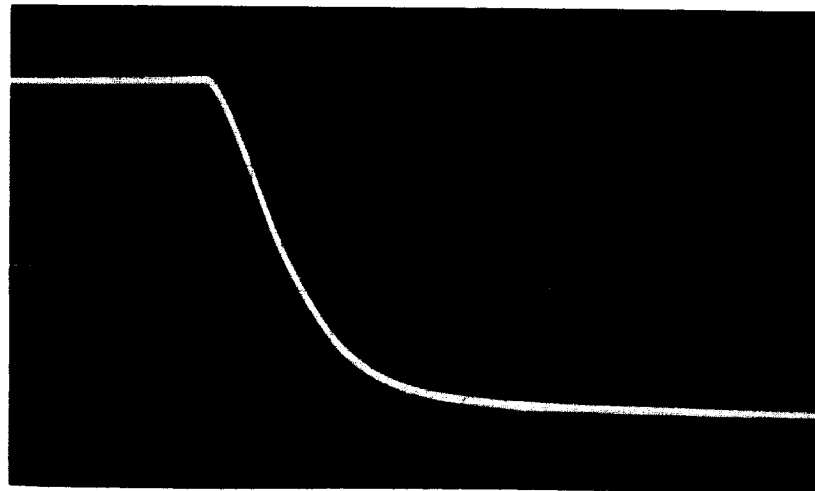
Along with Equation (15) of Section 3.3.3.2, Equation (34) provides an analytical description of the voltage regulator loop. The voltage regulator input filter, i.e., L4 and C5, are neglected in this analysis; and the second order character of Equation (34) is due to the output filter, i.e., L5, C6 and C7. The coefficients in Equation (34) are determined by the component part parameters as defined in Appendix B.

Experimentally, Equation (34) was checked by opening the feedback loop and causing τ to be fixed. A step was caused to occur in V_{in} , and the inverter output monitored. It was observed that the envelope of the 400 cps inverter output was practically identical to the controlled dc voltage, i.e., the voltage regulator output voltage, and the controlled dc was monitored as the inverter output. A typical response to a step input in V_{in} is shown in Figure 62. Neither the controlled dc nor the inverter output response to a step in V_{in} could be approximated by a second order expression such as Equation (34). The experiment was subsequently modified to the simple arrangement of Figure 63. It was repeated with CR151 in and out of the circuit, for different values of inverter load, and with the controlled dc opened from the power converters and a 5 Ω resistor serving as a load. Under no conditions could the response to a step in V_{in} be adequately approximated by a second order expression such as Equation (34). It was difficult to achieve a step function at V_{in} , which could account to some extent for V not responding as expected. But further simplifications of the experiment involving only a 6 volt supply, L5, C6, C7 and a



Output Line Current = 0.6a

Vertical Scale: 2 v per div.
Horizontal Scale: 1 ms per div.



Power Converters Replaced with 5 Ohm Resistive Load

Vertical Scale: 0.5 v per div.
Horizontal Scale: 1 ms per div.

Figure 62. Response of the Controlled dc Voltage to a Step Function in V_{in} with the Feedback Loop Opened

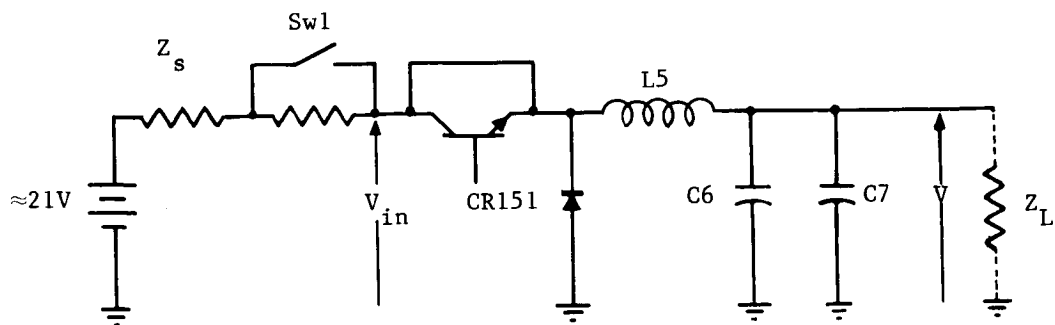


Figure 63. Schematic of Forward Loop Experiment

load resistor replacing the power converter yielded an improved step in V_{in} without a significant change in V . As a result of these experiments, it has been concluded that the most probable cause of the non-second order response in V is non-linear characteristics of $L5$.

The lack of an adequate analytical description of the forward portion of the voltage regulation loop required that the transient characteristics of the inverter be studied experimentally. Section 3.3.3.2 of this report describes the transient study in detail. Equations (12) and (13) of Section 3.3.3.2 do give accurate values for V and τ in steady-state operation and extensive analyses were performed in Section 3.3.3.2.

3.4 Design Stage Analysis Conclusions and Recommendations

The design of the static inverter is basically sound and, with minor exceptions noted below, employs good functional techniques and components having adequate ratings. The design is conservative, but not at the expense of weight or volume. This enhances both performance and life. Some specific recommendations are given below and some amplifying discussion follows.

- (1) Modify the coupling circuits from the diode OR gate configurations (elements 32 - 45) to resistive coupling (elements 32M - 45M). This modification allows the elimination of 100 diodes (CR1 - CR96 and CR141 - CR144) and requires the addition of 14 resistors (R1' - R14'). This recommendation results from the analysis presented

in Reference 3 which concluded that the modification gives improved performance and life. This modification also requires changing the values of resistors R1 - R14.

(2) Reduce the positive feedback in the magnetic amplifier circuit to a level such that the over-all transfer characteristic is linear. The basis for this recommendation are the analyses presented in Sections 3.3.3.2 and 3.3.4.15 which show that the very high gain currently employed introduces non-linearities with less predictable behavior and also decreases the static regulation and the stability capability due to the increased sensitivity of the output voltage to circuit parameters. Transient response characteristics were not observed to degrade with a decreased gain. A gain level corresponding to three feedback turns ($N_f = 3$) with the present values of R67 and R69 is adequate.

(3) Conduct further investigation of the pulse sequence generator performance. This recommendation is made in view of the uncertainty in the pulse sequence generator performance experienced throughout the project and especially the observed malfunctions described in Section 3.3.4.6. As described in Section 3.3.4.6, the most logical approach is a testing program to measure the pulse sequence generator performance under controlled conditions of input clock pulse amplitude, V_{cc} supply voltage, flip flop loads, and ambient temperature with the experiment designed to include several levels of each.

(4) Continue the use of redundant timing generator circuits in the timing section. Even though this gives only slight advantage in the predicted reliability (Section 3.3.1.1), the uncertainties in performance associated with the integrated circuits in the pulse sequence generator recommends redundancy to give added confidence not accountable in the analysis.

(5) Assess the criticality of the output transients which are generated during the switchover from one timing generator to the other. Both the momentary loss of output and the shift in frequency during the recovery period should be considered.

(6) Assess the significance of the observed transient response resulting from disturbances in input voltage and step changes in load and determine whether further investigation is necessary. This also applies to turn-on transients.

(7) Consider the feasibility of matching the temperature coefficients of resistors R73 and R75 and of close thermal coupling of these in the completed package. The basis for this recommendation is the output voltage sensitivity analysis in Section 3.3.3.2. Sensitivity to variations in both were found to be large and approximately equivalent but of different sign. With matched coefficients, drift due to temperature in one would offset that in the other.

- (8) Select and qualify, if available, a suitable diode to replace the two parallel reactive diodes in each half of the power converter circuits. Thus the twenty-four 1N645 diodes (CR111 - CR135) would be replaced with twelve of a different type. This recommendation is based on the component stress analysis in Section 3.3.1.3.
- (9) Replace C5 in the primary voltage regulator with a similar capacitor or a parallel combination of capacitors to achieve a higher ripple current rating. A single capacitor adequately rated for the expected ripple current is preferred.
- (10) Screen transistors Q19 - Q21 to ascertain a minimum value of h_{FE} of 20 at $V_{CE} = 1$ v, $I_C = 5$ amp and 25°C ambient temperature. In Section 3.3.4.16, it is concluded that h_{FE} for the 2N1937 must have a minimum value of 15.3 for this application while a minimum value of 10 is specified by the manufacturers. The larger h_{FE} provides an additional safety margin against degradation and uncertainties in the analysis.
- (11) Screen transistors Q36 - Q47 to ascertain a minimum value of h_{FE} of 15 at $V_{CE} = 1$ v, $I_C = 5$ amp and 25°C ambient temperature. It was concluded in Section 3.3.4.9 that the minimum value of h_{FE} should be ten (10) or greater to assure transistor saturation. Several assumptions were necessary in estimating the maximum peak value of I_C so that little safety margin is provided by an h_{FE} value of ten. The increased minimum gain provides additional safety margins against degradation and uncertainties in the analysis.
- (12) Screen transistors Q13 and Q14 during production of the inverter to require that the gain-bandwidth product, f_T , be greater than 5 Mc. This is based on the discovery and analysis of the thermal run-away failure mode during overload.
- (13) Lower the threshold at which the output line current activates the overcurrent protection loop. This reduces the likelihood of inverter failures during overload conditions due to thermal run-away of transistors Q13 and Q14 but is not recommended in lieu of screening the transistors as stated in recommendation 12. Reduction of the threshold, for example, from 1.4 amp line current to 1.3 amp would not interfere with the inverter performance during the normal operating mode (defined as the range from zero to 1.25 amp output line current).
- (14) Continue use of the modified circuit for providing the regulated 6 vdc to the timing section circuits. This eliminates several components and also the unnecessary power dissipation as described in Section 3.3.4.1.
- (15) Replace the zener diode (CR152) in the 20 vdc regulated supply with a unit having a higher wattage rating. In the component stress analysis of Section 3.3.1.3,

it was shown that the computed worst-case power requirement approaches 6.5 watts. Manufacturer's rating at 25°C ambient temperature is 10 watts and based on a 45% de-rating from this value for high temperature operation, the unit currently employed is inadequate.

Further discussion of conclusions with regard to specific areas of investigation is presented below.

Output Frequency

In recognition of proposed design changes in the primary oscillator circuits to improve frequency stability, only limited consideration was given to the output frequency. An abbreviated analysis of the primary oscillator circuits concluded that their design was adequate on the basis of application of parts. Frequency stability is dependent primarily on the frequency standards employed. An interesting anomaly discovered was the shift in oscillator frequency during its start-up period. Recommendation 5 cites the need for further consideration of this effect.

Output Voltage

Extensive investigations are described in Section 3.3.3.2 for the average three-phase output voltage. Observed performance with the inverter breadboard circuit over the specified range of load, input voltage and temperature resulted in acceptable performance, that is, the variations from the preset value were less than one volt. This accounts only for static regulation, excluding long term stability. Analytical investigations considered the combined effect of all important circuit parameter variations and revealed that variations outside the ± 1.0 vac requirements are possible. For the circuit parameter and input voltage variations assumed, output voltage standard deviations on the order of one volt were computed as realistic values. Sensitivity to variations in input voltage was computed to be less than 0.1% and agrees closely with breadboard circuit measurements. As anticipated, sensitivity of output voltage is greatest for variations of components in the voltage reference section, i.e., the voltage error detection circuit. These consist of resistors R73, R74, and R75 and zener diode CR147 as shown in Figure 50. Recommendation 7 cites an advantage of matching temperature coefficients of resistors R73 and R75 and locating them in similar thermal environments.

Recommendation 2 treats the problem of gain optimization for minimizing output voltage variations. The analysis in Section 3.3.3.2 did not provide conclusive evidence that a clear-cut optimum gain level exists but did show that no advantage is achieved by providing a magnetic amplifier gain near infinity as currently practiced. Actually, the recommendation is based more on the undesirability of introducing the

non-linear characteristics in the magnetic amplifier transfer characteristics in instrumenting the high gain.

Output Voltage Imbalance

Voltage imbalance was treated analytically with circuit equations for the output circuit. Investigations were primarily worst-case, assuming pessimistic values for circuit parameter variations and load imbalance and neglecting possible correlations of parameter values. For balanced load conditions, circuit parameter variations yielded worst-case imbalance values as large as six volts, about four times the 1.5 v requirement; however, in view of the large parameter variations assumed and of the fact that the uncorrelated worst-case conditions are unlikely, the results are not alarming. Computed sensitivities to one-at-a-time parameter variations did not yield any unbalance greater than one volt. Further analyses with more realistic parameter variations would probably reveal that requirements are met without difficulty.

Separate investigation revealed that with extremes of load unbalance, voltage imbalance requirements are not met. The worst-case computed was approximately six volts resulting when either two of the phase loads were 160 Ω (full load) and the other 1600 Ω (approximately no load). Further investigations could yield the maximum allowable load unbalance for assuring voltage imbalance requirements are met.

Output Phase Imbalance

Phase imbalance was investigated analytically with the output circuit equations. Phase imbalance is small due to the inherent manner of generating the output waveform and contributions result only from load imbalance and variations in output circuit parameters which are more critical to voltage imbalance. The worst-case calculations that yielded the large voltage imbalance yielded a worst-case phase imbalance of about 2.5 deg. Typical requirements assumed were 2.0 deg. On the basis of the pessimistic worst-case results, it is concluded that phase imbalance is acceptable.

Output Distortion

Output distortion was treated analytically with circuit equations for the power converter circuits and the output circuit. Output distortion for nominal inverter operation was computed to be about 1.5% which agrees closely with the measured distortion on the breadboard circuit. The analysis was primarily worst-case for investigating the possible sources of contribution to output distortion. The greatest contributions were variations in the output filter which cause less attenuation of harmonics. These contributions were insignificant. Output distortion during normal operation of the inverter is never more than 2.0% which is more than adequate when compared to the 5% requirement.

Power Dissipation

Total power dissipation was investigated experimentally by measuring input and output voltages and currents at different load conditions and ambient temperature environments and computing input and output powers for comparison. The inverter is optimally designed for supplying a reactive load of 250 volt-amperes with voltage leading current by 45 deg. The power dissipation for this load was determined to be 75 watts yielding an efficiency of 71%. The requirement of 70% minimum efficiency is satisfied for this load condition. For a resistive load the maximum dissipation at full load is 140 watts yielding an efficiency of 64%.

RF Interference

Because of analytical complexity in treating RF interference during design stage analysis, it was neglected in the analysis. This attribute is more feasible analyzed experimentally with experimental and prototype models of the complete package.

Transient Response

Transient response studies were focused on how disturbances such as transients on input voltage and step changes in load affect the output voltage amplitude. Attempts to treat the transient response analytically were unsuccessful due to the non-linear characteristics of the voltage regulation loop. Empirical studies revealed that the transient response of the output voltage is more significant than originally anticipated. Maximum deviations, i.e., the 400 cps voltage peak values, of 50 v were observed in response to simulated step changes in input voltage. This exceeds the assumed requirements of 8 v. Transient time, however, was always observed to be well below the 100 msec assumed requirement.

Measurements revealed that the voltage deviation is related to the time in the period of the output sine wave that the disturbance occurs. The dependence of the transient on types and magnitudes of disturbances was observed but not analyzed in detail. Recommendation 6 cites the desirability of further investigation of transient characteristics.

The particular disturbance caused by switching between redundant timing generator circuits was also briefly investigated. Voltage variations were much larger than anticipated with the output essentially disappearing for the equivalent of several 400 cps periods. Recommendation 5 cites the need for assessment of this effect. The anomaly in frequency observed during this transient is discussed above.

Turn-on Transients

Investigation of turn-on transients was limited to several observations at different load conditions. The overshoot and damping characteristics of the 400 cps

voltage waveform envelope are very similar to those observed for response to step changes in input voltage with the characteristics improving with increased load. Overshoot exceeds the assumed typical requirement of 15%; however, turn-on time is much less than the assumed typical requirement of 100 msec. Recommendation 6 cites the necessity of assessing the significance of these transients.

Turn-off Transients

Investigation of turn-off transients was limited to a single observation. Decay to zero occurs within 20 msec.

Six-volt Regulated Supply

Although the design of the original six-volt supply is adequate, Reference 2 suggested a simpler design that incorporated the same redundancy features, eliminated one failure mode that would probably result in inverter failure, and reduced power dissipation. The original six-volt supply was redesigned by the inverter design group, however, and no further consideration has been given the relative merits of the original design and that proposed in Reference 2.

The modified six-volt supply represents an improvement over the original design primarily because of its simpler configuration. It is not an optimum design for the present six-volt load, but the design can be readily optimized by changing R81 and R82 when the final six-volt load is known.

Electronic Switch

Since the turns ratios for T9 and T10 in the modified electronic switch were unknown, an analysis of the modified electronic switch was not possible. The circuit does not require a unique transformer design for satisfactory operation, however, and Section 3.3.4.2.2 illustrated satisfactory operation of the circuit for a particular transformer turns ratio. For the turns ratio used in the illustration, the design of the modified electronic switch is concluded to be satisfactory.

Primary Oscillator

Only limited consideration has been given the primary oscillator design since it is subject to replacement. Its frequency characteristics are determined by the characteristics of the crystal, and its amplitude characteristics are satisfactory. All of the components are adequately rated for their respective applications. The frequency variations of the crystal during start-up of this circuit were noted earlier.

Frequency Countdown Circuit

The frequency countdown circuit has a configuration recommended by the manufacturer for the SN511A networks. Although some difficulties have been experienced

in the breadboard model of the inverter with the SN511A flip flops, these were confined to the pulse sequence generator and none have occurred in the frequency countdown circuit. As reported in Section 3.3.4.4, SN511A flip flops that did malfunction in the pulse sequence generator were found to later function normally in the frequency countdown circuit. Consequently, the design of the frequency countdown circuit is satisfactory.

Clockpulse Amplifier

The design of the clockpulse amplifier is satisfactory. In Reference 2, the necessity for including the clockpulse amplifier in the static inverter was questioned and it was reported that the inverter had been operated with the clockpulse amplifier removed from the active timing generator. Further investigation and observation of failures in the pulse sequence generator, however, has demonstrated its necessity and the clockpulse amplifier design is satisfactory for this application.

Pulse Sequence Generator

The pulse sequence generator configuration is essentially identical to one recommended by the manufacturer of the SN511A networks. However, several breadboard malfunctions are attributed to malfunctions of the pulse sequence generator. These have not been explained and recommendation 3 suggests a test program to further investigate this effect. The SN511A characteristics are still not adequately understood and are obviously critical in this application. Since no difficulties were observed until after significant breadboard operation with the clockpulse amplifier temporarily removed, it is possible that the SN511A flip flops degraded during that period. All units were exposed from time to time to appreciable thermal and electrical stresses approaching their maximum ratings. With redundancy employed in the timing section, the design of the pulse sequence generator is considered acceptable.

Coupling Circuits

Conclusions with regard to recommended modifications are discussed in connection with the timing pulse amplifiers and the magnetic amplifier driver circuit.

Timing Pulse Amplifier

It has been recommended that the timing pulse amplifiers (TPA) and their associated coupling circuits be modified. From an analysis of the original TPA design, it was concluded that the TPA transistors did not have sufficient base drive to assure saturation for worst-case conditions. Consequently, a modification of the TPA's and their associated coupling circuits was proposed in Reference 3 that provided sufficient base drive to the TPA transistors and increased circuit reliability for

all expected conditions. Except for the insufficient base-drive current for worst-case conditions, the design of the original TPA's is satisfactory. The design of the modified circuit is also satisfactory in all respects.

Power Converters

Recommendation 8 cites the need for replacing the parallel reactive diodes in the power converters with a single diode. The paralleled diodes are inadequately rated to conduct the peak recurrent current for worst-case conditions. Also, a failure of one of the paralleled units in a shorted mode will result in a failure of the inverter, and a failure in an opened mode will double the stress on the remaining diode and greatly increase its likelihood of failure. Consequently, it is concluded that any diode failure will result in an inverter failure and the paralleled diodes are disadvantageous. It is recommended, therefore, that a single diode be selected to replace the paralleled 1N645's. The diode should be adequately rated to conduct the peak recurrent diode current, the average current, and block the peak voltage to be applied in the reverse direction.

In all other respects, the design of the power converters is satisfactory, although it was recommended that the power converter transistors be screened for a minimum h_{FE} .

Output Circuit

The design of the output circuit is satisfactory.

Voltage Error Detection Circuit

The design of the voltage error detection circuit is satisfactory. As a result of the sensitivity analysis discussed in Section 3.3.3.2, a recommendation has been made concerning the temperature coefficients and the thermal environment of R73 and R75.

Overcurrent Detection Circuit

The design of the overcurrent detection circuit is satisfactory. It was recommended, however, that the threshold level of the overcurrent detection circuit be lowered since it can be lowered without influencing the inverters normal mode of operation. Lowering the threshold level will enhance the ability of the overcurrent protection loops to protect the inverter in an overcurrent mode of operation.

20 vdc Regulated Supply

It was recommended that the wattage rating of CR152 in the 20 vdc regulated supply circuit be increased. In all other respects, the design of this element is satisfactory.

Magnetic Amplifier Drive Circuit

It was recommended that the design of the magnetic amplifier drive circuit and its associated coupling circuits be modified although the original design was concluded to be good. In Reference 3, a modification suggested for the TPA's and their associated coupling circuits was also recommended for the magnetic amplifier drive circuit since it results in an improved reliability over the original design.

Magnetic Amplifier

No changes are recommended for the magnetic amplifier for normal modes of inverter operation. In Section 3.3.4.15, however, it is noted that the transistors in the magnetic amplifier output circuit, i.e., Q13 and Q14, dissipate excessive power in an overcurrent mode of operation due to their slow switching rates; and Reference 2 discusses the frequently observed failure of these transistors. The component stress analysis of Section 3.3.1.3, which ignores the dissipation during switching, shows the power dissipation rating of Q13 and Q14 to be adequate, but it also concluded that the minimum f_{β} rating is inadequate. f_T is specified for the S2N2034A transistors to range between 1 Mc and 6 Mc. If Q13 and Q14 are selected by requiring that $f_T \geq 5$ Mc, f_{β} would be adequate and the failure described above would be unlikely to occur.

Primary Voltage Regulator

In Reference 2, it is concluded that C5 in the primary voltage regulator conducts excessive ripple current. It is estimated that the rms ripple current at full load will be approximately 6.4 a, 5.3 a of ripple current has been measured in C5, and the rated ripple current is 1.8 a. It is assumed that the input filter formed by L4 and L5 is essential to isolate the unregulated inverter input bus from the 9.6 kc demand of the primary voltage regulator and, therefore, C5 is an essential component to the static inverter. At 9.6 kc, C5 is approximately self-resonant and its critical parameter is the equivalent series resistance (ESR), not the actual capacitance. The permissible ripple current is determined by the heating effect of the ripple current in the ESR. It has been recommended that steps be taken to increase the rated ripple current.

Section 3.3.4.16 concluded that the gain of Q19 - Q21 in the primary voltage regulator is inadequate for this application, and screening has been recommended as a remedy for this inadequacy. Distribution data descriptive of the 2N1937 indicate that less than 10% of these transistors will have an h_{FE} value of 20 or less for the conditions of interest.

In all other respects, the design of the primary voltage regulator is adequate.

4.0 Later Stage Considerations

Design stage analyses as exemplified in Section 3.0 provide for solving many problems before the final package is designed and fabricated. This, as has been noted, allows corrective action at minimum cost. However, it is necessary to continue both analytical and empirical studies with the prototype equipment in order to account for the major influences of the package design. With electronic equipment, thermal influences are typically a major consideration, i.e., the operating temperature and the thermal interactions. Other notable differences from the breadboard model result from the circuit layout and RF interference.

The procedures developed and the sensitivities noted in the design stage studies can be directly extrapolated to the prototype equipment. These can be supplemented with thermal mapping, especially hot spot detection, and the detection of additional interactions. The test results with prototype models should be analyzed and compared to the previous results with particular attention to sensitive parameters. Tests for prototype equipment can be designed to obtain data which allows more accurate description of performance. The effort, at this level, can be much less than that during the design stage if that analysis was thorough.

During production, careful attention should be given to "foolish failures" caused by imperfect workmanship. Screening and testing procedures to eliminate "goofs" and techniques to minimize them should be sought. Attention should be given to the accumulation of operational experience with production items as this adds greatly to the knowledge of the equipment's reliability.

Some brief comments pertaining to the static inverter serve to illustrate typical design considerations for later stages.

4.1 Experimental Model

Experimental models of the complete inverter provide realistic models for testing and further study. Design and analysis techniques for the package design are less quantitative than for the circuit design effort and the designer must rely heavily on experience and standard practice.

The inverter circuitry will be completely enclosed by a metal housing primarily to suppress the radiated RF interference. In addition, RF filter capacitors are located on all external leads to attenuate conducted RF energy. Design for meeting RF interference requirements is facilitated by RF tests in which observed spectra can identify needed modifications in RF shielding or filter design. The circuit layout should provide adequate RF shielding of the timing section (at least those portions employing integrated circuits) from the control and conversion section

where heavy current switching occurs.

Because of the enclosure, temperature inside the housing will probably exceed the ambient temperature by a significant amount. Consequently, heat generation in the final package and heat conduction from the package must be considered for each different inverter application. Experimental measurements of internal ambient temperatures can be made at various locations within the package to check for operating conditions and especially for hot spots. Analytical techniques for performing thermal mapping are becoming popular and provide useful information for thermal design. These results, when appropriately verified with measurements from the experimental model provide more realistic thermal stresses of components for updating reliability predictions.

More realistic measures of performance can be obtained by experimental model testing than from analytical studies or breadboard testing during circuit design. In addition to experimental checks of all performance attributes, empirical models of important attributes can be very beneficial at this stage. For example, average three-phase voltage was identified in the circuit design analysis as an important attribute and the major interface characteristics that can influence it are input voltage variations, load level and the thermal environment. As described in Volume I, experiments can be conveniently designed to collect data for formulating a regression model such as

$$V_{out} = b_0 + b_1 V_{in} + b_2 I_{out} + b_3 T$$

where V is voltage, I is current, T is ambient temperature and the b's are the regression coefficients obtained empirically. This technique was demonstrated in the design analysis (see Section 3.3.3.2), but the model there had less significance since the thermal environment for the breadboard is not truly representative of that for the final packaged version.

Regression models can easily be made more sophisticated than the form presented above to include additional effects and higher order terms of second degree variations and interaction effects. Such models are useful as descriptions of performance for application considerations. Particularly when operating conditions for specific missions are known, their substitution into the model provides a prediction of the attribute behavior.

For the inverter it is recommended that modeling efforts be pursued for average three-phase voltage and output frequency. As an off-the-shelf equipment, the accompanying prediction models for these attributes will provide useful information to

the systems designer and will promote its selection for application.

4.2 Production

The production process for the inverter is governed primarily by purchase specifications with quality assurance tests and inspection providing the quality control. Well-written specifications are a major contribution to reliability. Typically, such specifications are prepared by updating specifications from similar earlier model equipment to incorporate new design features and requirements.

For the static inverter, specifications of an earlier model inverter were revised to reflect changes in power capability and environment [Ref. 4] and employed as design requirements in the reliability analysis. With additional modifications, these specifications can provide the necessary control during production. Some facets of the design that should be included in the specifications are:

- (1) transient operation for start-up, turn-off, and response to external disturbances of the load and dc input,
- (2) overcurrent protection circuit operation, especially in terms of the threshold output current level at which the circuit is activated,
- (3) extension of the environmental requirements to encompass all possible operational conditions,
- (4) allowable load imbalance and power factor for acceptable inverter operation,
- (5) effects of load starting conditions on inverter operation, and
- (6) special design or fabrication provisions.

Item 6 would include explicit requirements with regard to such factors as screening, circuit layout, and housing design. Specifically, it may be desired to eliminate the manual adjustment of the output voltage provided by R74 by using a fixed voltage divider consisting of R73 and R75 with explicit requirements stated for the selection of the resistors for individual production units. Provision could also be made for optimizing the power factor correction for specific applications by output filter adjustment if different missions require different loads. Statement of requirements for voltage regulation loop gain selection of individual units could be made to account for differences in magnetic amplifier cores. Such requirements should be made explicit commensurate with the findings from the design analyses.

5.0 Conclusions with Regard to the Analysis Approach

This analysis of the static inverter is based on models which correlate performance attributes for the equipment with the various factors that influence its operation. Both analytical and empirical modeling techniques were employed. Emphasis was on design stage analyses and on techniques that improve performance. Certain design problems were identified with this approach which had not been detected by conventional studies. These include

- (1) gain adjustment of the voltage regulation loop for minimizing output voltage variations,
- (2) magnitude of output voltage transients caused by external disturbances and their dependence on time of disturbance,
- (3) momentary disappearance of the output voltage during switchover from one redundant timing channel to the other,
- (4) shift in output frequency during switchover from one redundant timing channel to the other,
- (5) relative sensitivities of output voltage to the numerous circuit parameter variations that influence it, and
- (6) effects of circuit parameter correlations on output voltage.

Some typical results which could have been obtained with conventional methods but which were picked up in this study are the

- (7) redesign of timing generator output coupling circuits to reduce the number of parts required,
- (8) identification of the most sensitive parameters for output voltage variations,
- (9) assurance that output distortion and output voltage and phase imbalance is acceptable, and
- (10) effects of input current modulation.

Finally, other results obtained from conventional methods with little or no contribution from new analytical methods were

- (11) redesign of the six-volt regulated supply,
- (12) discovery of an over-stressed capacitor in the input filter,
- (13) discovery of a thermal run-away failure mode of transistors in the magnetic amplifier circuit, and
- (14) determination of power dissipation and efficiency.

The above lists are not inclusive but are presented as typical results. It is concluded that this analysis offered definite improvements in the inverter design.

The probabilistic modeling concepts from the previous contract effort (contract NASw-334) led to the methods used, but the full extent of the modeling methods was not employed. This results from the impracticality of completely modeling complex systems. In this design analysis, the approach was directed toward prediction of the success probability; however, the practical result (frequently made on the basis of comparing designs) is usually obtained long before a realistic success probability can be computed. This does not imply that the concepts promoted are invalid, but rather that they are beneficial in directing the effort. The assembly of techniques described in Volume I of this report is a logical follow-on to the previous effort. Tools are described for instrumenting the concepts in a practical context. The static inverter analysis demonstrated that in many cases elementary techniques employing simple models are adequate for resolving specific problems. A typical example is the elimination of 100 diodes from the coupling circuit which was based on elementary design analyses. Sophistication is beneficial in resolving more complex problems, as for example the gain adjustment in the voltage regulator.

With regard to design reliability efforts, the most significant output from this effort is the recognition of the interrelationship of the various reliability analysis tasks. These are discussed in Section 2.0 of Volume I of this report giving evidence that a reliability methodology is evolving. Some of this interrelationship is reflected in the static inverter analysis; however, much of it evolved from the analysis and is thus not reflected in the methods used. As an example, the failure modes and effects analyses followed extensive modeling studies. It is now apparent that this should precede the application of other methods in order to identify the modes of equipment behavior to be investigated in the other efforts. Performance variation analyses, stress analyses, and reliability prediction are described in proper perspective in Volume I.

6.0 References

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8. "Analysis of a Magnetic Amplifier Used in the 250VA Static Inverter," Project Memorandum EU-172-16, December 15, 1964, Research Triangle Institute, Durham, North Carolina.
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10. Series 51 Application Report for Solid Circuit Semiconductor Networks, Texas Instruments, Inc., Dallas, Texas, 1962.

APPENDIX A

Output Circuit Equations

These equations are presented to supplement the analysis of the output circuit for voltage and phase imbalance in Section 3.3.1.4. A complete schematic diagram of the output circuit is presented in Figure 49. For the purpose of deriving the following equations, the simplified version shown in Figure A-1 was used. In addition to the obvious assumptions in simplifying the circuit, the effects of the loads provided by the voltage error detection circuit and the over-current detection transformers and associated circuit are neglected. These were analyzed and shown to be insignificant [Ref. 2]. In Figure A-1, the ideal voltage sources V'_{ab} , V'_{bc} , and V'_{ca} and the resistances r_{ab} , r_{bc} , and r_{ca} represent the three-phase interconnection of the secondary windings of the six output transformers.

The equations for the four loops defined in Figure A-1 are

$$z_{11} I_1 - z_{12} I_2 - z_{13} I_3 - z_{14} I_4 = V'_{ab} \quad (A-1)$$

$$-z_{21} I_1 + z_{22} I_2 - z_{23} I_3 - z_{24} I_4 = V'_{bc} \quad (A-2)$$

$$-z_{31} I_1 - z_{32} I_2 + z_{33} I_3 - z_{34} I_4 = V'_{ca} \quad (A-3)$$

$$-z_{41} I_1 - z_{42} I_2 - z_{43} I_3 + z_{44} I_4 = 0 \quad (A-4)$$

where

$$z_{11} = \frac{1}{Y_{12} + j\omega C_1} + r_{ab} + j\omega(L_1 + L_2), \quad (A-5)$$

$$z_{22} = \frac{1}{Y_{23} + j\omega C_2} + r_{bc} + j\omega(L_2 + L_3), \quad (A-6)$$

$$z_{33} = \frac{1}{Y_{31} + j\omega C_3} + r_{ca} + j\omega(L_3 + L_1), \quad (A-7)$$

$$z_{44} = z_{41} + z_{42} + z_{43}, \quad (A-8)$$

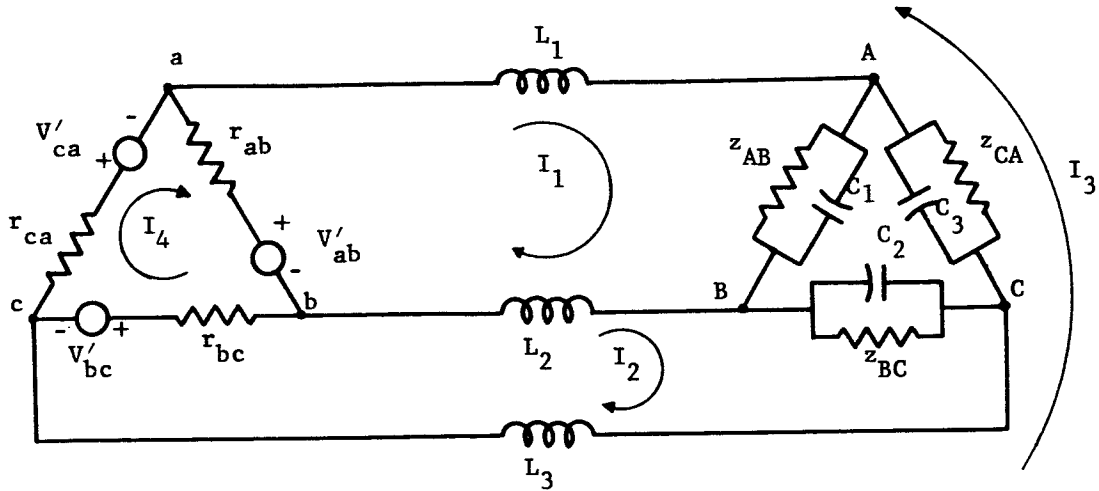


Figure A-1. Simplified Version of the Output Circuit for Analysis

$$z_{12} = z_{21} = j\omega L_2, \quad (\text{A-9})$$

$$z_{13} = z_{31} = j\omega L_1, \quad (\text{A-10})$$

$$z_{14} = z_{41} = r_{ab}, \quad (\text{A-11})$$

$$z_{23} = z_{32} = j\omega L_3, \quad (\text{A-12})$$

$$z_{24} = z_{42} = r_{bc}, \quad (\text{A-13})$$

$$z_{34} = z_{43} = r_{ca}, \quad (\text{A-14})$$

$$Y_{12} = \frac{1}{z_{AB}}, \quad (\text{A-15})$$

$$Y_{23} = \frac{1}{z_{BC}}, \quad (\text{A-16})$$

and

$$Y_{31} = \frac{1}{z_{CA}}. \quad (\text{A-17})$$

All voltages and impedances in the above equations are functions of complex frequency, $j\omega$. Specifically, for the input voltages

$$V'_{ab} = |V'_{ab}| e^{jn\omega_1 t}, \quad (A-18)$$

$$V'_{bc} = |V'_{bc}| e^{jn(\omega_1 t - \frac{2\pi}{3})}, \quad (A-19)$$

and

$$V'_{ca} = |V'_{ca}| e^{jn(\omega_1 t - \frac{4\pi}{3})}, \quad (A-20)$$

where $n = 1, 2, \dots$ and $\omega_1/2\pi = 400$ cps, the fundamental frequency. Load impedances are expressed by

$$z_{AB} = |z_{AB}| e^{j\theta_{AB}}, \quad (A-21)$$

$$z_{BC} = |z_{BC}| e^{j\theta_{BC}}, \quad (A-22)$$

and

$$z_{CA} = |z_{CA}| e^{j\theta_{CA}}, \quad (A-23)$$

where the θ 's represent the angle of the reactive components.

For the analysis described in Section 3.3.1.4, the above equations were programmed for general solution by digital computer solution of the current I_1 , I_2 , I_3 and I_4 . Inputs to the program were values of the resistances, capacitances, inductances, and specified characteristics of the input voltages and load impedances. The outputs of interest from the program were programmed for computation using the following equations.

Generator Currents

$$I_{ba} = I_1 - I_4 \quad (A-24)$$

$$I_{cb} = I_2 - I_4 \quad (A-25)$$

$$I_{ac} = I_3 - I_4 \quad (A-26)$$

Generator Voltages

$$V_{ab} = V'_{ab} - I_{ba} r_{ba} \quad (A-27)$$

$$V_{bc} = V'_{bc} - I_{cb} r_{bc} \quad (A-28)$$

$$V_{ca} = V'_{ca} - I_{ac} r_{ca} \quad (A-29)$$

Line Currents

$$I_{aA} = I_1 - I_3 \quad (A-30)$$

$$I_{bB} = I_2 - I_1 \quad (A-31)$$

$$I_{cC} = I_3 - I_2 \quad (A-32)$$

Load Voltages

$$V_{AB} = \frac{I_1}{Y_{12} + j\omega C_1} \quad (A-33)$$

$$V_{BC} = \frac{I_2}{Y_{23} + j\omega C_2} \quad (A-34)$$

$$V_{CA} = \frac{I_3}{Y_{31} + j\omega C_3} \quad (A-35)$$

Load Currents

$$I_{AB} = V_{AB} Y_{12} \quad (A-36)$$

$$I_{BC} = V_{BC} Y_{23} \quad (A-37)$$

$$I_{CA} = V_{CA} Y_{31} \quad (A-38)$$

Phase Balance Voltages

$$\Delta V_A = |V_{CA}| - |V_{AB}| \quad (A-39)$$

$$\Delta V_B = |V_{AB}| - |V_{BC}| \quad (A-40)$$

$$\Delta V_C = |V_{BC}| - |V_{CA}| \quad (A-41)$$

Phase Differences

$$\Delta \phi_A = (\text{Ang. of } V_{CA}) - (\text{Ang. of } V_{AB}) \quad (A-42)$$

$$\Delta \phi_B = (\text{Ang. of } V_{AB}) - (\text{Ang. of } V_{BC}) \quad (A-43)$$

$$\Delta \phi_C = (\text{Ang. of } V_{BC}) - (\text{Ang. of } V_{CA}) \quad (A-44)$$

APPENDIX B

Definitions of Terms Used in the Voltage Regulation Loop Analysis

The following equations and definitions are presented as additional information for the analysis in Section 3.3.3.2:

$$A_o = \frac{1}{L_R C_R} \quad (B-1)$$

$$A_1 = \frac{6K_1}{K_2 C_R} \quad (B-2)$$

$$B_o = -\frac{V_{ce,s}}{K_2 L_R C_R} \quad (B-3)$$

$$B_1 = \frac{1}{K_2 L_R C_R T} \quad (B-4)$$

$$C_1 = -\frac{N R_e}{V K_\phi} (\phi'_K + \phi_S) + \frac{R_e T}{K'_\phi} + \frac{N R_e N V_z}{V R_{c1}} \quad (B-5)$$

$$C_2 = -\frac{3}{\pi} \sqrt{2} \times \frac{N R_e N}{V R_{c1}} \quad (B-6)$$

$$x = \frac{R_{73} + \alpha R_{74}}{R_{73} + R_{74} + R_{75}} \quad (B-7)$$

$$k = \frac{R_e}{K_\phi} \quad (B-8)$$

$$R_e = \left[\frac{N_{c1}^2}{R_{c1}} + \frac{N_{sh}^2}{R_s} \right]^{-1} \quad (B-9)$$

$$K'_\phi = \frac{K_\phi}{1 - \left(\frac{R_{67}}{R_{67} + R_{69}} \right) \left(\frac{K N_f N}{T R_g} \right)} \quad (B-10)$$

$$\phi'_K = \frac{\phi'_K + \frac{R_{67}}{R_{67} + R_{69}} \frac{K_{\phi} N_f}{R_g'} \left[\frac{N_g \phi_S}{T} - V_g \right]}{1 - \left(\frac{R_{67}}{R_{67} + R_{69}} \right) \left(\frac{K_{\phi} N_f N_g}{TR_g'} \right)} \quad (B-11)$$

$$R_{c1} = R_w + x(1 - x)(R_{73} + R_{74} + R_{75}) \quad (B-12)$$

$$K_1 = \frac{\sqrt{2} \cdot 577}{90\pi} (\cos \theta_S) \left| j\omega C + \frac{1}{z_L} \right| \quad (B-13)$$

$$K_2 = \frac{90 \sqrt{2}}{741} \left| 1 + (j\omega C + \frac{1}{z_L})(R_S + j\omega 3L) \right| \quad (B-14)$$

$$+ \frac{\sqrt{2} \cdot 577}{90\pi} R_p (\cos \theta_S) \left| j\omega C + \frac{1}{z_L} \right|$$

$$\theta_S = \text{Ang.} \left[3j\omega L + R_S + \frac{1}{j\omega C + z_L^{-1}} \right] \quad (B-15)$$

The symbols in the above equations are defined as follows:

- C - capacitance in the inverter output filter (C1, C2, C3)
- C_R - capacitance in the primary voltage regulator (C6, C7)
- j - $\sqrt{-1}$
- K_φ - slope of the magnetic amplifier core reset characteristics, reset flux versus mmf
- L - inductance in the inverter output filter (L1, L2, L3)
- L_R - inductance in the primary voltage regulator (L5)
- N_{c1} - number of turns in the magnetic amplifier control winding
- N_f - number of turns in the magnetic amplifier feedback winding
- N_g - number of turns in the secondary windings of the gate voltage supply transformer (T7) for the magnetic amplifier
- N_{sh} - number of turns in the magnetic amplifier shorted winding
- R_g' - combined series resistance of one branch of the magnetic amplifier gate circuit during the ON period (with reference to Figure 55, this includes the resistances of the secondary windings of the gate voltage supply transformer; the magnetic amplifier gate and

feedback windings, and the resistor; and the equivalent resistances of the diode and base-emitter junctions at the conduction levels.)

- R_j - resistance of resistor R_j
- R_p - resistance of the primary windings in the inverter output transformers (T1-T6)
- R_s - resistance of the secondary windings in the inverter output transformers (T1-T6)
- R_{sh} - resistance of the shorted winding in the magnetic amplifier
- R_w - resistance of the magnetic amplifier control winding
- T - half-cycle period of the 4.8 kc magnetic amplifier gate excitation (104.17 μ sec)
- V_{ces} - collector-to-emitter saturation voltage for the transistors (Q36-Q47) in the power converter stages
- V_g - zero-to-peak amplitude of the magnetic amplifier gate supply voltage
- V_z - zener voltage of reference zener (CR147) in the voltage error detection circuit
- z_L - impedance of the inverter output load
- α - relative position of the arm of potentiometer R74
- ϕ_K - intercept of the magnetic amplifier core reset characteristics, reset flux versus mmf
- ϕ_s - saturation flux level of the magnetic amplifier core
- ω - fundamental frequency of the inverter output ($\omega/2\pi = 400$ cps.)

APPENDIX C

Failure Modes and Effects Summary

Table C-I contains a listing of component failure modes and effects for the original version of the inverter circuit as described in Section 3.3.1.2. The effects of circuit modification on the failure mode and effects analysis are summarized in Table C-II. To facilitate the tabulation the following abbreviations are used.

<u>Symbol</u>	<u>Definition</u>
DO	degraded output
DP	degraded performance
SO DTR	sustained operation due to redundancy
F	failure
FC	failure occurs but is conditioned on the normal operating state of the circuit
FD	failure occurs but is delayed
FP	failure is possible but depends on accompanying effect on other parts
ID	increased distortion
LR	loss in voltage regulation
NL	normal load conditions for the inverter
O	open
OL	overload conditions for the inverter
OP	overload protection provided
PD	possible damage to inverter (applies only during OL)
S	short
SO	sustained operation
VI	voltage unbalance

TABLE C-I

Summary of Component Failure Modes and
Effects for the Original Circuit

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
Resistors:				
R1-R12	46-51	0	F	FP
R13, R14	62	S	FD	FP
		0	F	F
R15-R26	46-51	S	FD	FD
		0	S0	S0
R27, R28	21	both	F	FP
R29	60	0	S0	S0
				NL: S0
				OL: OP
		S	F	NL: S0
R30-R41	52-57			OL: PD
		0	F	FP
R42, R43	28, 29	S	F	FP
		both	F	S0 DTR
R45, R46	28, 29	0	F	S0 DTR
R47, R48	28, 29	S	FD	S0 DTR
		0	FP	S0 DTR
R49, R50	28, 29	S	F	S0 DTR
		0	S0	S0
R51	60	S	F	S0 DTR
		0	S0	S0
R52-R54	22, 23	S	F	F
		0	F	S0 DTR
R55	23	S	FD	S0 DTR
		0	F	S0 DTR
R56, R57	22, 23	S	FP	S0 DTR
		both	F	S0 DTR

TABLE C-I (Continued)

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
R58	22	O	F	SO DTR
		S	FP	SO DTR
R59	22	O	F	SO DTR
		S	FD	SO DTR
R60	60	O	F	NL: SO
				OL: PD
		S	SO	NL: SO
				OL: OP
R61	60	O	F	NL: SO
				OL: PD
		S	SO	NL: SO
				OL: OP
R62, R63	62	O	SO	SO
		S	F	F
R64, R65	63	O	FP	FP
		S	F	F
R67	63	O	FP	FP
		S	DP	DP-LR
R68	64	O	SO	SO
		S	F	F
R69	63	O	DP	DP-LR
		S	FP	FP
R70	64	O	F	F
		S	SO	SO
R71	64	O	SO	SO
		S	F	F
R72	61	both	F	F
R73	59	both	F	F
R74 (Potentiometer) For all terminal pairs	59	O	F	F
		S	FP	FP
R75, R76	59	both	F	F
R77-R80	21	O	SO	SO
		S	F	SO DTR

TABLE C-I (Continued)

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
R81, R82	21	0	S0 DTR	S0
		S	F	F
R83, R84	21	0	S0	S0
		S	FC	FC
Transistors:				
Q1-Q12	46-51	all	F	FP
Q13, Q14	63	all	F	F
Q15, Q16	21			
B-E		both	S0	S0
C-E and C-B		0	S0	S0
		S	S0 DTR	S0
Q17, Q18	62	all	F	F
Q19-Q21	64			
B-E		S	F	F
		0	S0 DTR	S0
C-E and C-B		S	F	F
		0	S0 DTR	S0
Q22-Q27	22, 23	all	F	S0 DTR
Q28-Q29	28, 29	all	F	S0 DTR
Q35	60			
B-E		both	F	NL: S0
				OL: PD
C-E and C-B		0	F	NL: S0
				OL: PD
		S	F	F
Q36-Q47	52-57	all	F	F
Capacitors:				
C1-C3	58	0	DP	D0-ID
		S	F	F
C4	60	0	S0	S0
		S	F	F
C5-C7	64	0	DP	D0-ID
		S	F	F

TABLE C-I (Continued)

Component	Element Location	Failure Modes	Effect	
			Immediate Circuit	Inverter Output
C8	61	0	S0	S0
		S	F	F
C9, C10	22, 23	0	S0	S0
		S	F	S0 DTR
Inductors:				
L1-L3	58	0	DP	D0-ID and VI
		S	DP	D0-ID
L4, L5	64	0	F	F
		S	DP	D0-ID
Diodes:				
CR1-CR96	34-45	0	S0	S0 DTR
		S	S0	S0 DTR
CR97, CR98	62	0	F	F
		S	F	F
CR99-CR104	59	0	DP	DP
		S	F	F
CR105-CR110	60	0	S0	S0
		S	F	F
CR111-CR134	52-57	both	F	F
CR135-CR138	22, 23	both	F	S0 DTR
CR139, CR140	21	both	FC	F
CR141-CR144	32-33	both	FC	F
CR145-CR146	21	0	FC	F
		S	S0 DTR	S0
CR147	59	both	F	F
CR148	60	0	F	NL: S0
				OL: PD
		S	DP	DP
CR149, CR150	63	0	DP	DP
		S	F	F
CR151	64	both	F	F
CR152	61	both	F	F

TABLE C-I (Continued)

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
CR153, CR154	63	both	F	F
Transformers:				
T1-T6	52-57			
All primary windings		both	F	F
All secondary windings		0	DP	DO-VI
		S	F	F
Any primary to any secondary winding		S	F	F
T7	62			
All terminal pairs		both	F	F
T8	63			
All primary windings		both	F	F
Secondary centertap terminal		0	F	F
Other secondary terminals		0	DP	DP-LR
Any secondary terminal pair		S	F	F
Any primary to any secondary winding		S	F	F
T9, T10	22, 23			
All terminal pairs		both	F	S0 DTR
T11-T13	58			
Primary windings		0	F	DO-VI
		S	S0	S0
Secondary windings		both	S0	S0
Primary to secondary windings		S	S0	S0
T14-T19	46-51			
All terminal pairs		both	F	F
Flip-flops:				
FF1A-FF6A and FF1B-FF6B	30, 31			
Terminals 1, 3-7, 10		0	F	S0 DTR
Terminal 2		0	S0	S0
Terminal 8, 9		0	F	DO-ID and VI

TABLE C-I (Continued)

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
All terminal pairs except 2 to 7		S	F	S0 DTR
Terminals 2 to 7		S	S0	S0
FF7A, FF7B	30, 31			
Terminals 1-3, 6-10		0	F	S0 DTR
Terminals 4, 5		0	S0	S0
All terminal pairs except: 4 to 5, 7, 8, 10 5 to 7, 8, 10 and 8 to 10		S	F	S0 DTR
For above exceptions		S	S0	S0
FF8A-FF10A and FF8B-FF10B	26, 27			
Terminals 1, 3-7, 9, 10		0	F	S0 DTR
Terminals 2, 8		0	S0	S0
All terminal pairs except: 1 to 6, 8 2 to 7 5 to 9, 10 6 to 8 9 to 10		S	F	S0 DTR
For above exceptions		S	S0	S0
FF11A, FF11B	26, 27			
Terminals 1, 3-10		0	F	FC
Terminal 2		0	S0	S0
All terminal pairs except: 1 to 6 2, 3 to 7 5 to 10		S	F	FC
Terminal pairs 1 to 6, 2 to 7, and 5 to 10		S	S0	S0
Terminal pairs 3, 4 to 7		S	F	S0 DTR
FF12A, FF12B	26, 27			
Terminals 1, 3-8, 10		0	F	S0 DTR
Terminals 2, 9		0	S0	S0

TABLE C-I (Continued)

<u>Component</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effect</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
All terminal pairs except:		S	F	S0 DTR
1 to 6, 8				
2 to 7				
5 to 9, 10				
6 to 8				
9 to 10				
For above exceptions		S	S0	S0

TABLE C-II

Summary of Component Failure Modes and
Effects Changes for the Modified Circuit

<u>Components</u>	<u>Element Location</u>	<u>Failure Modes</u>	<u>Effects</u>	
			<u>Immediate Circuit</u>	<u>Inverter Output</u>
R81, R82 (Reapplied)	21M-1	both	F	SO DTR
	21M-2			
CR145, CR146 (Reapplied)	21M-1	both	F	SO DTR
	21M-2			
CR139, CR140 (Deleted)	21			
Q15, Q16 (Deleted)	21			
R27, R28 (Deleted)	21			
R83, R84 (Deleted)	21			
C16, C17 (Added)	22M, 23M	O	SO	SO
		S	F	SO DTR
R1-R12 (Reapplied)	34M-45M	O	F	FC
		S	F	SO DTR
R1'-R12' (Added)	34M-45M	O	F	FC
		S	F	SO DTR
CR1-CR96 (Deleted)	34-45			
R13, R14 (Reapplied)	32M, 33M	O	F	FC
		S	FC	FC
R13', R14' (Added)	32M, 33M	O	F	FC
		S	FC	FC
CR141-CR144 (Deleted)	32, 33			

APPENDIX D

Equations for Harmonic Distortion Analysis

Computing formulas for performing the harmonic distortion analysis, as described in Section 3.3.1.4, are developed and presented below. This modeling approach relates the inverter output distortion back to circuit parameters in the power converters. Due to circuit symmetry it is necessary to consider only a single phase of the three-phase output.

The model formulation is illustrated by the flow diagram shown in Figure D-1. Circuit equations for the power converter permit computation of the exciting voltages, the V_{iU} 's and the V_{iL} 's, for the primary windings of the output transformers. The resulting rectangular waves across the secondary windings of the output transformer are summed to obtain the step levels A_1, \dots, A_{12} of the stepped waveform as shown in Figure D-2. For a given set of step levels, the waveform is resolved, by Fourier series analysis, into amplitudes of the fundamental and harmonic components, i.e., the $E_i(n)$'s. As shown in the Appendix of Reference 1, the contribution to distortion caused by higher frequency harmonics is negligible, therefore the computation was limited to values for n of 40 and less. Distortion D_s of the stepped waveform is computed for comparison to that of the ideal waveform. The distortion D_o of the inverter output waveform is determined from the amplitudes, the $E_o(n)$'s of the waveform components where these are derived from the $E_i(n)$'s by applying the appropriate gain characteristics of the output filter. The equations in the model are developed below.

The circuit diagram for converter No. 1 is shown in Figure 45. The diagram for power converter Nos. 2-6 are identical except for different component designations. To obtain an expression for the exciting voltage of the output transformer assume that transistor Q36 is ON, transistor Q37 is OFF, and that the inverter output load is such that diodes CR111 and CR112 are not required to conduct. Considering the similar state for the other power converters, the transformer exciting voltage for the upper portion of the i -th circuit is

$$V_{piU} = V_C - R_{iU}I - V_{siU}, \quad (D-1)$$

where the subscripts are defined as

p denotes the exciting voltage in the transformer primary winding,

i denotes the i -th converter circuit ($i = 1, \dots, 6$),

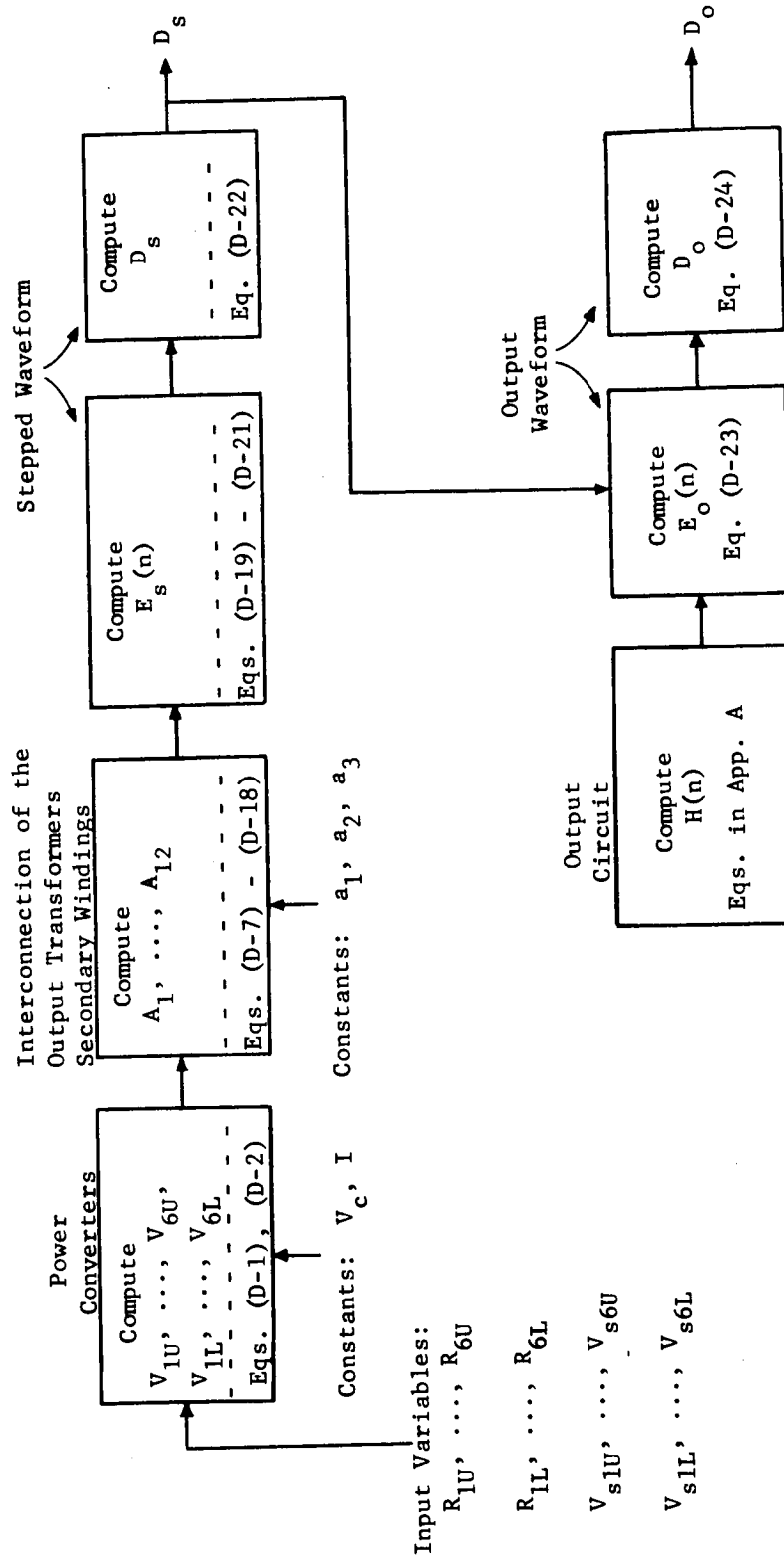


Figure D-1. Flow Diagram for the Output Distortion Model

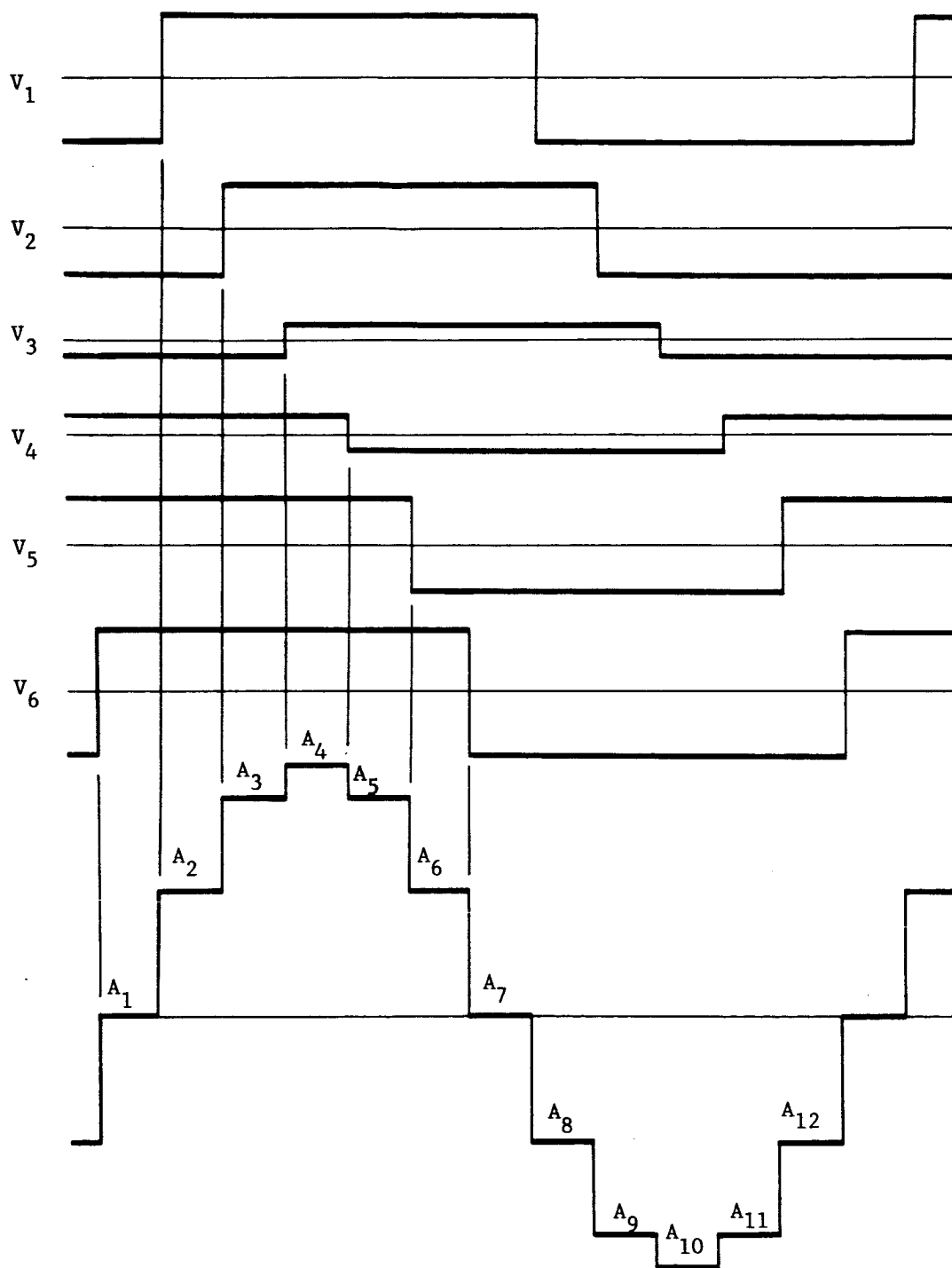


Figure D-2. Synthesis Process for the Stepped Waveform

U denotes the upper portion of the inverter circuit,

C denotes the controlled dc input from the primary voltage regulator, and

s denotes the collector to emitter saturation condition for the transistors.

In (D-1) R represents the resistance of the upper half of the transformer primary winding, and since it can vary among the circuits, is a source of contribution to output distortion. Similarly, V_{siU} , representing the transistor collector to emitter saturation voltage, is a source of contribution to distortion. Furthermore, I represents the average value of current during the state of the circuit assumed. It was shown in Reference 2 that the current is not constant which can give rise to time variations in the voltage. Observations of the stepped waveform using the breadboard circuit with the output filter disconnected revealed that these effects are essentially averaged out in the summation process so that the waveform steps are adequately represented by constant voltages; hence a fixed value of I is used.

Similarly, the transformer exciting voltage for the lower portion of the i-th circuit is

$$V_{piL} = V_C - R_{iL}I - V_{siL} , \quad (D-2)$$

where the subscript denotes the lower portion of the circuit and the other subscripts are as defined above.

The interconnections of the secondary windings of the six output transformers and the resulting summation of the rectangular waveforms to obtain a stepped waveform was described in detail in Reference 1. Figure D-2 contains a simplified illustration of the summation process for reference herein. The voltages of the rectangular waves are derived directly from the transformer exciting voltages above through the appropriate terms ratios

$$a_1 = \frac{N_1}{N_p} = \frac{370}{180} , \quad (D-4)$$

$$a_2 = \frac{N_2}{N_p} = \frac{276}{180} , \quad (D-5)$$

$$a_3 = \frac{N_3}{N_p} = \frac{94}{180} , \quad (D-6)$$

where N_p is the number of turns in the primary winding and N_j , ($j = 1, 2, 3$) is the number of turns in the appropriate secondary winding. The resulting voltage levels

across the secondary windings appear as $\pm a_j V_{iU}$ or $\pm a_j V_{iL}$ depending on the particular converter circuit considered. The algebraic combination of these voltage levels to obtain the stepped waveform is summarized by the following equations:

$$A_1 = -a_1 V_{1U} - a_2 V_{2U} - a_3 V_{3U} + a_3 V_{4U} + a_2 V_{5U} + a_1 V_{6U} \quad (D-7)$$

$$A_2 = +a_1 V_{1L} - a_2 V_{2U} - a_3 V_{3U} + a_3 V_{4U} + a_2 V_{5U} + a_1 V_{6U} \quad (D-8)$$

$$A_3 = +a_1 V_{1L} + a_2 V_{2L} - a_3 V_{3U} + a_3 V_{4U} + a_2 V_{5U} + a_1 V_{6U} \quad (D-9)$$

$$A_4 = +a_1 V_{1L} + a_2 V_{2L} + a_3 V_{3L} + a_3 V_{4U} + a_2 V_{5U} + a_1 V_{6U} \quad (D-10)$$

$$A_5 = +a_1 V_{1L} + a_2 V_{2L} + a_3 V_{3L} - a_3 V_{4L} + a_2 V_{5U} + a_1 V_{6U} \quad (D-11)$$

$$A_6 = +a_1 V_{1L} + a_2 V_{2L} + a_3 V_{3L} - a_3 V_{4L} - a_2 V_{5L} + a_1 V_{6U} \quad (D-12)$$

$$A_7 = +a_1 V_{1L} + a_2 V_{2L} + a_3 V_{3L} - a_3 V_{4L} - a_2 V_{5L} - a_1 V_{6L} \quad (D-13)$$

$$A_8 = -a_1 V_{1U} + a_2 V_{2L} + a_3 V_{3L} - a_3 V_{4L} - a_2 V_{5L} - a_1 V_{6L} \quad (D-14)$$

$$A_9 = -a_1 V_{1U} - a_2 V_{2U} + a_3 V_{3L} - a_3 V_{4L} - a_2 V_{5L} - a_1 V_{6L} \quad (D-15)$$

$$A_{10} = -a_1 V_{1U} - a_2 V_{2U} - a_3 V_{3U} - a_3 V_{4L} - a_2 V_{5L} - a_1 V_{6L} \quad (D-16)$$

$$A_{11} = -a_1 V_{1U} - a_2 V_{2U} - a_3 V_{3U} + a_3 V_{4U} - a_2 V_{5L} - a_1 V_{6L} \quad (D-17)$$

$$A_{12} = -a_1 V_{1U} - a_2 V_{2U} - a_3 V_{3U} + a_3 V_{4U} + a_2 V_{5U} - a_1 V_{6L} \quad (D-18)$$

The amplitude of each frequency component of the stepped waveform is

$$E_s(n) = \sqrt{a_n^2 + b_n^2}, \quad n = 1, 2, \dots, 40 \quad (D-19)$$

where a_n and b_n are the standard coefficients in a Fouries series expansion. For the periodic waveform in Figure D-2 the coefficients equate to

$$a_n = \frac{\sin \frac{\pi n}{12}}{\pi n} \sum_{k=1}^{12} A_k \cos \frac{\pi n}{6} (k - \frac{1}{2}) \quad (D-20)$$

and

$$b_n = \frac{\sin \frac{\pi n}{12}}{\pi n} \sum_{k=1}^{12} A_k \sin \frac{\pi n}{6} (k - \frac{1}{2}), \quad (D-21)$$

where A_k is the voltage level of the k-th step.

Relative distortion of a waveform is defined in general as the ratio of the rms value of the harmonic content to the rms value of the fundamental component. Since the analysis is limited to frequencies of $n = 40$ and less, the distortion for the unfiltered waveform is computed by

$$D_s = \frac{\sqrt{\sum_{n=2}^{40} E_s^2(n)}}{E_s(1)}. \quad (D-22)$$

The amplitudes of the frequency components in the inverter output waveform are obtained by applying the appropriate gain values of the output filter to the components obtained for the stepped waveform, as

$$E_o(n) = H(n)E_s(n) \quad (D-23)$$

where $H(n)$ is the gain of the output filter at frequency n . Values of $H(n)$ for the analysis were obtained by solution of the circuit equations presented in Appendix A.

Using the frequency components obtained with (D-23), the output distortion is computed by

$$D_o = \frac{\sqrt{\sum_{n=2}^{40} E_o^2(n)}}{E_o(1)} . \quad (D-24)$$

Use of the above equations in the analysis for output distortion is described in Section 3.3.1.4.

APPENDIX E

Component Stress Analysis

This appendix tabulates the results of the component stress analyses discussed in Section 3.3.1.3 of this report. Tables E-I through E-V provide a direct comparison between the component ratings and the worst-case power dissipations, voltages and currents expected in each component. Estimates of worst-case stresses are made assuming worst-case purchase parameter values for the components and with all variables at their worst-case extreme limits.

A summary of the results of stress analyses for resistor applications in the static inverter is shown in Table E-I. The nominal power dissipation rating for 25°C is listed in the first power dissipation column. The derated value for 125°C, the maximum temperature environment expected for the static inverter, is given in the second column. The worst-case column tabulates expected power dissipation in the resistors under worst-case conditions. Attention is called to those resistors for which the estimated worst-case power dissipation equals or exceeds 75% of the 125°C rating. These are R70, 80%; and R83 and R84, 90%.

The voltage ratings of all resistors were also compared with the maximum voltage requirements. In every case, the rated voltage was a minimum of 25% greater than the maximum voltage difference expected in the inverter circuitry.

TABLE E-I

Stress Analysis for Resistor Application

Part No.	Type	Element Location	Power Dissipation (Watts)		
			Nominal 25°C Rating	125°C Rating	Worst-case
Original Circuit:					
R1-R12	RN55C	46-51	0.25	0.1	< 0.05
R13, R14	RN55C	62	0.25	0.1	< 0.05
R15-R26	RN55C	46-51	0.25	0.1	< 0.001
R27, R28	RN55C	21	0.25	0.1	0.0007
R29	RN55C	60	0.25	0.1	< 0.04
R30-R41	RH5	52-57	5	—	< 2.4
R42-R50	RN55C	28, 29	0.25	0.1	< 0.035
R51	RN55C	60	0.25	0.1	< 0.03
R52-R54	RN55C	22, 23	0.25	0.1	< 0.05
R55-R58	RN55C	22, 23	0.25	0.1	< 0.06
R59	RN55C	22	0.25	0.1	< 0.05
R60	RN55C	60	0.25	0.1	< 0.05
R61	RN55C	60	0.25	0.1	< 0.02
R62, R63	RN55C	62	0.25	0.1	< 0.0001
R64, R65	RW69V	63	3	2.2	< 0.04
R67	RW69V	63	3	2.2	< 0.2
R68	RW69V	64	3	2.2	< 0.4
R69	RW69V	63	3	2.2	< 0.2
R70	RE65G	64	10	7	5.6
R71	RW69V	64	3	2.2	< 1.4
R72	RE70G	61	15	10.5	< 4.5
R73	RW69V	59	3	2.2	< 0.1

TABLE E-I (continued)

Part No.	Type	Element Location	Power Dissipation (Watts)		
			Nominal 25°C Rating	125°C Rating	Worst-case
R74	49M	59	1.5	—	< 0.1
R75	243E	59	5	3.7	< 1.4
R76	243E	59	5	—	< 1.8
R77-R80	RN55C	22, 23	0.25	0.1	< 0.0002
R81, R82	RE65G	21	10	7	< 4.6
R83, R84	RN55C	21	0.25	0.1	0.09
Modifications:					
R1-R12 (Reapplied)	RN55C	34M-45M	0.25	0.1	< 0.07
R1'-R12' (Added)	RN55C	34M-45M	0.25	0.1	< 0.07
R13-R14 (Reapplied)	RN55C	32M, 33M	0.25	0.1	< 0.07
R13'-R14' (Added)	RN55C	32M, 33M	0.25	0.1	< 0.07
R27, R28 (Deleted)		21			
R81, R82 (Reapplied)	RE70G	21M-1, 21M-2	15	10	5
R83, R84 (Deleted)		21			

Table E-II summarizes the results of stress analyses for diode applications in the static inverter. The stresses considered are the power dissipation, reverse voltage, and forward current. The worst-case power dissipation values correspond to products of maximum currents and voltages. In the worst-case, forward current column, the maximum recurrent peak current is tabulated as a worst-case value when the recurrent peak value and the average value differ. Table E-II lists as a requirement for CR111-CR134, for example, a worst-case forward current of 2.1 amperes. Section 3.3.4.9 of this report shows that value to be the recurrent peak requirement for the conditions assumed in the analysis of elements 52-57. The average current requirement is 0.325 amperes. CR111-CR134 are the only diodes listed in Table E-II for which any rating is inadequate. These diodes and their requirements are discussed in Section 3.3.4.9. All tabulated worst-case power dissipations are less than 45% the 25°C rating, and all voltages and currents are less than 75% of the rated values except in the case of CR111-CR134.

TABLE E-II

Stress Analysis for Diode Application

Part No.	Type	Element Location	Power Dissipation		Reverse Voltage		Forward Current		
			Nominal	Worst-case (watts)	Rated (volts)	Worst-case (volts)	Recurrent		
			25°C Rating (watts)				Peak (amp.)	Average (amp.)	Worst-case (amp.)
Original Circuit:									
CR1-CR96	S1N645	34-45	0.6	< 0.01	225	~ 0	1.25	0.4	< 0.01
CR97, CR98	S1N645	62	0.6	< 0.12	225	40	1.25	0.4	< 0.1
CR99-CR104	S1N645	59	0.6	0.024	225	< 163	1.25	0.4	< 0.02
CR105-CR110	S1N645	60	0.6	< 0.05	225	< 15	1.25	0.4	< 0.1
CR111-CR134	S1N645	52-57	0.6	0.220	225	< 50	1.25	0.4	2.1
CR135-CR138	S1N645	22, 23	0.6	< 0.01	225	< 15	1.25	0.4	< 0.01
CR139, CR140	S1N645	21	0.6	0.065	225	< 7.9	1.25	0.4	0.065
CR141-CR144	S1N645	32, 33	0.6	< 0.012	225	< 1	1.25	0.4	< 0.01
CR149, CR150	S1N1204A	63	12	< 2.7	400	< 5	50	12.0	< 3
CR151	S1N1204A	64	12	5	400	30	50	12.0	4.2
CR153, CR154	1N3730	63	> 0.75	< 0.2	100	< 12	> 0.7	> 0.7	< 0.2
Modification:									
CR1-CR96 (Deleted)									
CR135-CR138 (Reapplied)	S1N645	22M, 23M	0.6	< 0.026	225	~ 0	1.25	0.4	< 0.026
CR139-CR144 (Deleted)									

The results of the stress analyses for zener diode applications, as summarized in Table E-III, show these components to be adequately rated for their respective applications with one exception. It is pointed out that CR152 which is nominally rated to dissipate 10 watts at 25°C can be required to dissipate approximately 6.5 watts under worst-case conditions. No recommendations are made by the manufacturer for derating CR152; and it is likely that, when derated for 125°C, the rated and required power dissipation capabilities will have an unsatisfactory ratio of values.

TABLE E-III

Stress Analysis for Zener Diode Application

Part No.	Type	Element Location	Power Dissipation		Zener Voltage		Zener Current	
			Nominal 25°C Rating (watts)	Worst-case (watts)	Rated (volts)	Tolerance (volts)	Rated (amp.)	Worst-case (amp.)
Original Circuit:								
CR145, CR146	1N3017B	21	1	0.36	7.5	± 0.4	0.135	0.046
CR147	S1N3156A	59	0.4	0.2	8.4	< ± 0.9	—	< 0.02
CR148	S1N3156A	60	0.4	0.1	8.4	< ± 0.9	—	< 0.01
CR152	S1N2084B	61	10	6.5	20	± 1	0.480	0.26
Modification:								
CR145, CR146 (Reapplied)	S1N2970B	21M-1	10	1.52	6.8	± 0.34	1.5	< 0.21

The results of the stress analyses for transistor applications are summarized in Table E-IV. The stresses considered are the usual ones, i.e., power dissipation, voltages and currents. In addition, Table E-IV also tabulates the specified minimum f_{β} and the application frequency. Most of the transistors in the static inverter are used in switching applications, and in computing the power dissipation in these transistors it was assumed that the switching times were so short as to make dissipation during switching negligible. Generally, this assumption is valid if f_{β} is greater than the application frequency by a factor of ten (10) or more. The computations yielding the required power dissipation also assumed that adequate base drive was provided to assure that the transistors were saturated ON during their ON periods.

From Table E-IV, it is concluded that the transistors are adequately rated for their respective applications with the following exceptions. The worst-case V_{CEO} for Q1-Q12, Q13, Q14, and Q24-Q27 (modified) is 86% of the rated BV_{CEO} . It is pointed out in Section 3.3.4, however, that the parameter of interest is actually BV_{CER} ; and it is concluded in each of these cases that the BV_{CEO} rating is adequate. Also, for Q13 and Q14, the minimum f_{β} is not greater than the application frequency by a factor of ten (10). The results of an inadequate minimum f_{β} for Q13 and Q14 are discussed in Section 3.3.4.15. For all other cases, the worst-case power dissipations are less than 75% of the rated dissipation at 125°C, worst-case voltages and currents are less than 75% the rated values, and f_{β} is greater than ten (10) times the application frequency.

Generally, the assumption of sufficient base current to assure saturation of the transistor switches is valid. Two potential exceptions are Q1-Q12 and Q19-Q21. These potential difficulties are discussed in Section 3.3.4.7 and Section 3.3.4.16.

TABLE E-IV

Stress Analysis for Transistor Application

Part No.	Type	Element Location	Power Dissipation			Voltage				Current		Frequency			
			Nominal 25°C Rating (watts)	125°C Rating (watts)	Worst-case (watts)	BV _{CEO}		BV _{EB0}		I _C	I _B	min. f _β (kc)	application (kc)		
						Rated (volts)	Worst-case (volts)	Rated (volts)	Worst-case (volts)						
Original Circuit:															
Q1-Q12	S2N2034A	46-51	8.5	3.5	< 0.085	70	60	10	< 1	3	0.10	1	< 0.01	10	0.4
Q13, Q14	S2N2034A	63	8.5	3.5	< 0.18	70	60	10	< 1	3	0.32	1	< 0.2	10	4.8
Q15, Q16	S2N2034A	21	8.5	3.5	< 0.15	70	7.9	10	< 1	3	0.15	1	0.012	10	dc
Q17, Q18	S2N2102	62	0.5	0.3	< 0.05	65	40	7	< 1	0.5	< 0.1	> 0.015	< 0.01	800	9.0
Q19-Q21	2N1937	64	> 150	> 9	< 3.3	80	30	6	< 1	20	< 5.5	10	< 3	180	9.6
Q22, Q23	S2N1132	22, 23	0.6	0.3	< 0.12	35	< 7.5	5	3	0.6	0.075	> 0.01	< 0.005	—	dc
Q24-Q27	S2N718A	22, 23	0.5	0.2	< 0.012	65	< 15	7	< 1	0.5	0.012	> 0.015	< 0.005	800	0.4
Q28, Q29	S2N718A	28, 29	0.5	0.2	< 0.036	65	7.2	7	< 1	0.5	< 0.005	> 0.015	< 0.005	800	4.8
Q35	S2N718A	60	0.5	0.2	< 0.01	65	< 22	7	< 1	0.5	< 0.01	> 0.015	< 0.001	800	dc
Q36-Q47	2N3432	52-57	> 150	> 5	< 2.5	200	< 50	25	< 5	7.5	< 3	≈ 5	< 0.8	100	0.4
Modification:															
Q15, Q16 (Deleted)															
Q22, Q23 (Reapplied)	2N3204	22M, 23M	8.75	—	< 0.16	80	30	—	≈ 5	—	0.163	—	< 0.001	—	dc
Q24-Q27 (Reapplied)	S2N2034A	22M, 23M	8.5	3.5	< 0.05	70	60	10	< 1	3	0.018	1	< 0.01	10	0.4

*When f_T is quoted in specifications, f_{β} is approximated as $f_T/100$. This corresponds to a β of 100 and a 6db/oct decay.

A summary of the results of stress analyses for capacitor applications in the static inverter is shown in Table E-V. The stresses considered are applied voltage and ripple current or ripple voltage. The table shows all components to be applied well within their rated capabilities with the exception of C5. The excessive ripple current in C5 is discussed in Section 3.3.4.16.

TABLE E-V

Stress Analysis for Capacitors

Part No.	Type	Element Location	Voltage		Peak Applied (volts)	Ripple Current		Ripple Voltage 125°C	
			Nominal dc 25°C Rating (volts)	125°C dc Rating (volts)		Rms Rating	Worst-case Rms	Rms Rating 10 kc	Worst-case Rms
C1-C3	118P...T4	58	400	400	< 165	—	—	> 0.15	< 0.1
C4	350D...S2	60	35	—	< 10	—	—	—	—
C5	202D...A4	64	45	30	< 25	1.8	≈ 6.4	—	—
C6, C7	202D...A4	64	45	30	< 22	1.8	≈ 1.1	—	—
C8	350D...S2	61	35	—	< 22	—	—	> 0.15	< 0.05
C9, C10	350D...S2	21	15	—	< 7	—	—	> 0.05	< 0.02

APPENDIX F

Static Inverter Parts List

I. Original Circuit

<u>Circuit Component No.</u>	<u>Description</u>	<u>Manufacturer</u>	<u>Mil Type or Manuf. Part No.</u>	<u>Element Location</u>
Resistors:				
R1-R12	392 Ω , 1/4w., $\pm 1\%$		RN55C6190F	46-51
R13, R14	301 Ω , 1/4w., $\pm 1\%$		RN55C3010F	62
R15-R26	1.5k, 1/4w., $\pm 1\%$		RN55C1501F	46-51
R27-R28	1.5k, 1/4w., $\pm 1\%$		RN55C1501F	21
R29	619 Ω , 1/4w., $\pm 1\%$		RN55C6190F	60
R30-R41	5 Ω , 5w., $\pm 3\%$	Dale	RH5	52-57
R42, R43	1.5k, 1/4w., $\pm 1\%$		RN55C1501F	28, 29
R44 (not used)				
R45, R46	1k, 1/4w., $\pm 1\%$		RN55C1001F	28, 29
R47, R48	475 Ω , 1/4w., $\pm 1\%$		RN55C4750F	28, 29
R49, R50	10k, 1/4w., $\pm 1\%$		RN55C1002F	28, 29
R51	10k, 1/4w., $\pm 1\%$		RN55C1002F	60
R52-R59	2k, 1/4w., $\pm 1\%$		RN55C2001F	22, 23
R60	1k-5k(selective) 1/4w.		RN55	60
R61	267 Ω , 1/4w., $\pm 1\%$		RN55C2670F	60
R62, R63	2.67k, 1/4w., $\pm 1\%$		RN55C2671F	62
R64, R65	40 Ω , 3w., $\pm 3\%$	Sprague	RW69	63
R66 (not used)				
R67	150 Ω , 3w., $\pm 3\%$	Sprague	RW69	63
R68	5 Ω , 3w., $\pm 3\%$	Sprague	RW69	64
R69	0.1k-1k(selective) 3w., $\pm 3\%$	Sprague	RW69	63
R70	1 Ω , 10w., $\pm 3\%$	Dale	RE65G1R00	64
R71	680 Ω , 3w., $\pm 3\%$	Sprague	RW69	64
R72	33 Ω , 15w., $\pm 3\%$	Dale	RE70G33R0	61
R73	1k-1.5k(selective) 3w., $\pm 3\%$	Sprague	RW69	59
R74	Variable, 200 Ω , 1.5w.	Clarostat	49M9200	59
R75	20k, 5w., $\pm 3\%$	Sprague	243E2032	59

Static Inverter Parts List (continued)

I. Original Circuit (continued)

<u>Circuit Component No.</u>	<u>Description</u>	<u>Manufacturer</u>	<u>Mil Type or Manuf. Part No.</u>	<u>Element Location</u>
R76	15k, 5w., $\pm 3\%$	Sprague	243E1532	59
R77-R80	7.5k, 1/4w., $\pm 1\%$		RN55C7501F	21
R81, R82	200 Ω , 10w.	Dale	RE65G2000	21
R83, R84	619 Ω , 1/4w., $\pm 1\%$		RN55C6190F	21
Transistors:				
Q1-Q12		Silicon Trans.	S2N2034A	46-51
Q13, Q14		Silicon Trans.	S2N2034A	63
Q15, Q16		Silicon Trans.	S2N2034A	21
Q17, Q18		RCA	S2N2102	62
Q19-Q21		Texas Instr.	2N1937	64
Q22, Q23		Texas Instr.	2N1132	22, 23
Q24-Q27		General Elec.	S2N718A	22, 23
Q28, Q29		General Elec.	S2N718A	28, 29
Q30-Q33		General Elec.	S2N718A	24, 25
Q35		General Elec.	S2N718A	60
Q36-Q47		Westinghouse	2N3432	52-57
Capacitors:				
C1-C3	2 μ f, 400V, $\pm 10\%$	Sprague	118P20594T4	58
C4	33 μ f, 35V, $\pm 10\%$	Sprague	350D336X9035	60
C5-C7	1000 μ f, 45V	Sprague	202D108X9045A4	64
C8	47 μ f, 35V	Sprague	350D476X9035	61
C9, C10	150 μ f, 15V	Sprague	350D157X9015	22, 23
Inductors:				
L1-L3		MSFC	R1159	58
L4		MSFC	R1073	64
L5		MSFC	R1074	64
Diodes:				
CR1-CR96		G.E. or T.I.	S1N645	34-45
CR97, CR98		G.E. or T.I.	S1N645	62
CR99-CR104		G.E. or T.I.	S1N645	59
CR105-CR110		G.E. or T.I.	S1N645	60
CR111-CR134		G.E. or T.I.	S1N645	52-57
CR135-CR138		G.E. or T.I.	S1N645	22, 23

Static Inverter Parts List (continued)

I. Original Circuit (continued)

<u>Circuit Component No.</u>	<u>Description</u>	<u>Manufacturer</u>	<u>Mil Type or Manuf. Part No.</u>	<u>Element Location</u>
CR139, CR140		G.E. or T.I.	S1N645	21
CR141-CR144		G.E. or T.I.	S1N645	32-33
CR145, CR146	Zener	Motorola	S1N3017B	21
CR147	Zener	Motorola	1N3156A	59
CR148	Zener	Motorola	1N3156A	60
CR149, CR150		Bendix	S1N1204A	63
CR151		Hughes	HF3C	64
CR152	Zener	Motorola	S1N2084B	61
CR153, CR154			1N3730	63
Transformers:				
T1-T6		MSFC	R1213	52-57
T7		MSFC	R1030	62
T8		MSFC	R1029	63
T9, T10		MSFC	R1191	22, 23
T11-T13		MSFC	R1158	58
T14-T19		MSFC	R1020	46-51
Integrated Circuits:				
FF1A-FF6A and FF1B-FF6B	Flip-flop	Texas Instr.	SN511A	30, 31
FF7A and FF7B	NAND-NOR gate	Texas Instr.	SN514A	30, 31
FF8A-FF12A and FF8B-FF12B	Flip-flop	Texas Instr.	SN511A	26, 27

II. Modifications

<u>Circuit Component No.</u>	<u>Description</u>	<u>Manufacturer</u>	<u>Mil Type or Manuf. Part No.</u>	<u>Element Location</u>
Resistors:				
R1-R8 (Reapplied)	$582\Omega^*$, 1/4w., $\pm 1\%$		RN55C	34M-41M
R1' -R8' (Added)	$582\Omega^*$, 1/4w., $\pm 1\%$		RN55C	34M-41M
R9, R10 (Reapplied)	$476\Omega^*$, 1/4w., $\pm 1\%$		RN55C	42M, 43M
R9', R10' (Added)	$476\Omega^*$, 1/4w., $\pm 1\%$		RN55C	42M, 43M

* Nominal values represent values computed in Reference 3.

Static Inverter Parts List (continued)

II. Modifications (continued)

<u>Circuit Component No.</u>	<u>Description</u>	<u>Manufacturer</u>	<u>Mil Type or Manuf. Part No.</u>	<u>Element Location</u>
R11, R12 (Reapplied)	$582\Omega^*$, 1/4w., $\pm 1\%$		RN55C	44M, 45M
R11', R12' (Added)	$582\Omega^*$, 1/4w., $\pm 1\%$		RN55C	44M, 45M
R13, R14 (Reapplied)	$412\Omega^*$, 1/4w., $\pm 1\%$		RN55C	32M, 33M
R13', R14' (Added)	$412\Omega^*$, 1/4w., $\pm 1\%$		RN55C	32M, 33M
R27, R28 (Deleted)				
R81, R82 (Reapplied)	114 Ω , 15w.	Dale	RE70G1140	21M-1, 21M-2
R83, R84 (Deleted)				
Transistors:				
Q15, Q16 (Deleted)				
Q22, Q23 (Reapplied)		STC	2N3204	22M, 23M
Q24-Q27 (Reapplied)		STC	2N2034A	22M, 23M
Capacitors:				
C9, C10 (Reapplied)	150 μ f, 15V	Sprague	350D157X9015	21M-1, 21M-2
C16, C17 (Added)	0.33 μ f, $\pm 10\%$	Sprague	350D334X9010A2	22M, 23M
Diodes:				
CR1-CR96 (Deleted)				
CR139-CR144 (Deleted)				
CR145, CR146 (Reapplied)	Zener	Motorola	S1N2970B	21M-1, 21M-2

* Nominal values represent values computed in Reference 3.

APPENDIX G

Observed Failures

Observed failures with the static inverter breadboard circuit are listed below. Some of these were discussed and referenced in the main text of this report. Not all failures reported imply a design discrepancy, e.g., the first one listed pertains to a failure inadvertently induced with a test probe. Failures purposely induced to observe failure effects are not included. The failures are as follows:

- (1) Failure: Transformer T14 and transistor Q2.

Location: Timing pulse amplifier (see Figure 43).

Symptom: Excessive distortion and voltage imbalance in the inverter output.

Remarks: This failure resulted when a test probe was inserted into the collector terminal socket of Q1 causing it to remain spread. This caused an open circuit in the collector circuit of Q1 when it was replaced, and as a result, T14 saturated and collector current increased to an excessive value in Q2 causing Q2 and T14 to fail. Fuses were installed at the center tap dc input of transformers T14 through T19 for future protection.

- (2) Failure: Magnetic amplifier gate winding open.

Location: Magnetic amplifier circuit (see Figure 55).

Symptom: Observed as open during breadboard assembly.

Remarks: This was a failure of a solder joint that probably occurred during handling. The unit was repaired in-house and used in the breadboard until the failure occurred several weeks later during operation. The symptom for the second failure was an excessively high output voltage. The second failure probably resulted also from further handling. The magnetic amplifier was replaced with a new unit for further operation and the failure did not reoccur during the program.

- (3) Failure: Zener diode CR152.

Location: 20 volt dc regulated supply (see Figure 52).

Symptom: No inverter output.

Remarks: The diode failed in a shorted mode. The cause of this failure is unknown.

- (4) Failure: SN511A flip-flop.

Location: Pulse sequence generator.

Symptom: The inverter would not operate with the timing generator that contained the failed unit.

Remarks: The failed SN511A unit was identified by its heatbuckled package. The unit was opened and found to be severely damaged by heat. The failure cause is unknown.

(5) Failure: Transistors Q13 and Q14 and transformer T8.

Location: Magnetic amplifier circuit (see Figure 55).

Symptom: No inverter output.

Remarks: This failure occurred with the inverter operating at 100°C, 25 vdc input, and a 1.5 amp. resistive load. Subsequent investigation identified a region in which Q13 and/or Q14 would consistently fail due to thermal run-away. This failure is discussed in Section 3.3.4.15 and Reference 2.

(6) Failure: Six SN511A flip-flops.

Location: Pulse sequence generator.

Symptom: The inverter would not operate with the timing generator that contained the failed units.

Remarks: Several of the failed units were opened for inspection. In the opened units, the deposited aluminum connectors from the clock pulse terminal to the two capacitors were opened and the capacitors were short-circuited. This failure occurred when the inverter was placed in a low temperature chamber. A 28 vdc supply was located in close proximity to the clock pulse lead which was being monitored, and it is possible that the two leads made contact causing the failure. Except for this possibility, there is no apparent reason for this failure.

(7) Failure: Timing section.

Symptom: Inverter inoperative.

Remarks: Both redundant timing generators were observed to function erratically. Cleaning all of the SN511A and SN514A printed circuit cards with alcohol and "touching up" the solder joints restored both timing generators to normal operation.

(8) Failure: Transistor Q28.

Location: Clockpulse amplifier (see Figure 38).

Symptom: The inverter would not operate with the timing generator that contained the defective unit.

Remarks: The failure cause is unknown. Normal operation resumed when the transistor was replaced with a spare unit.

(9) Failure: Transistor Q14.

Location: Magnetic amplifier circuit (see Figure 55).

Symptom: No magnetic amplifier output.

Remarks: This failure resulted from thermal run-away of Q14; however, it occurred under special test conditions. When the failure occurred, the inverter had been operating for approximately four hours with the magnetic amplifier output disconnected from the primary voltage regulator. With the inverter output disabled in this manner, the magnetic amplifier was operating with maximum output modulation which probably caused the failure of Q14.

(10) Failure: Zener diode CR147.

Location: Voltage error detection circuit (see Figure 50).

Symptom: Excessively low output voltage.

Remarks: CR147 had a zener voltage of 7.6 volts instead of its rated 8.4 volts. This failure occurred while the zener voltage of CR147 was being measured with a Hewlett Packard 412A voltmeter (isolated). The defective unit was replaced and operation resumed normally.

(11) Failure: SN511A flip-flops.

Location: Pulse sequence generator.

Symptom: Imbalance in the inverter output voltage and eventual failure of a timing pulse amplifier (indicated by blown fuse in the dc input to the center taps of transformers T14-T19).

Remarks: This failure occurred on numerous occasions and is discussed in Section 3.3.4.6. Initially, the discrepancy appears as an assymetry in the timing pulses from the pulse sequence generator. This results in an unbalanced drive to the timing pulse amplifier with the eventual fuse failure occurring because of the excessive collector current in the timing pulse amplifier transistors. As described in Section 3.3.4.6, the cause is unresolved.